ETM39E-03

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# *Application Manual*

## Real Time Clock Module

# RA8803SA

SEIKO EPSON CORPORATION

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# Contents

For automotive I²C-Bus Interface Real-time Clock Module

# RA8803SA

- Features built-in 32.768 kHz DTCXO, High Stability.
- Supports I²C-Bus's high speed mode (400 kHz)
- Alarm interrupt function for day, date, hour, and minute settings
- Fixed-cycle timer interrupt function
- Time update interrupt function (Seconds, minutes)
- 32.768 kHz output with OE function (FOE and FOUT pins)
- Auto correction of leap years (from 2000 to 2099)
- Wide interface voltage range: 2.2 V to 5.5 V
- Wide time-keeping voltage range:1.6 V to 5.5 V
- Low current consumption: 0.75μA / 3 V (Typ.)
- Time synchronization function by 1PPS(*) signal input

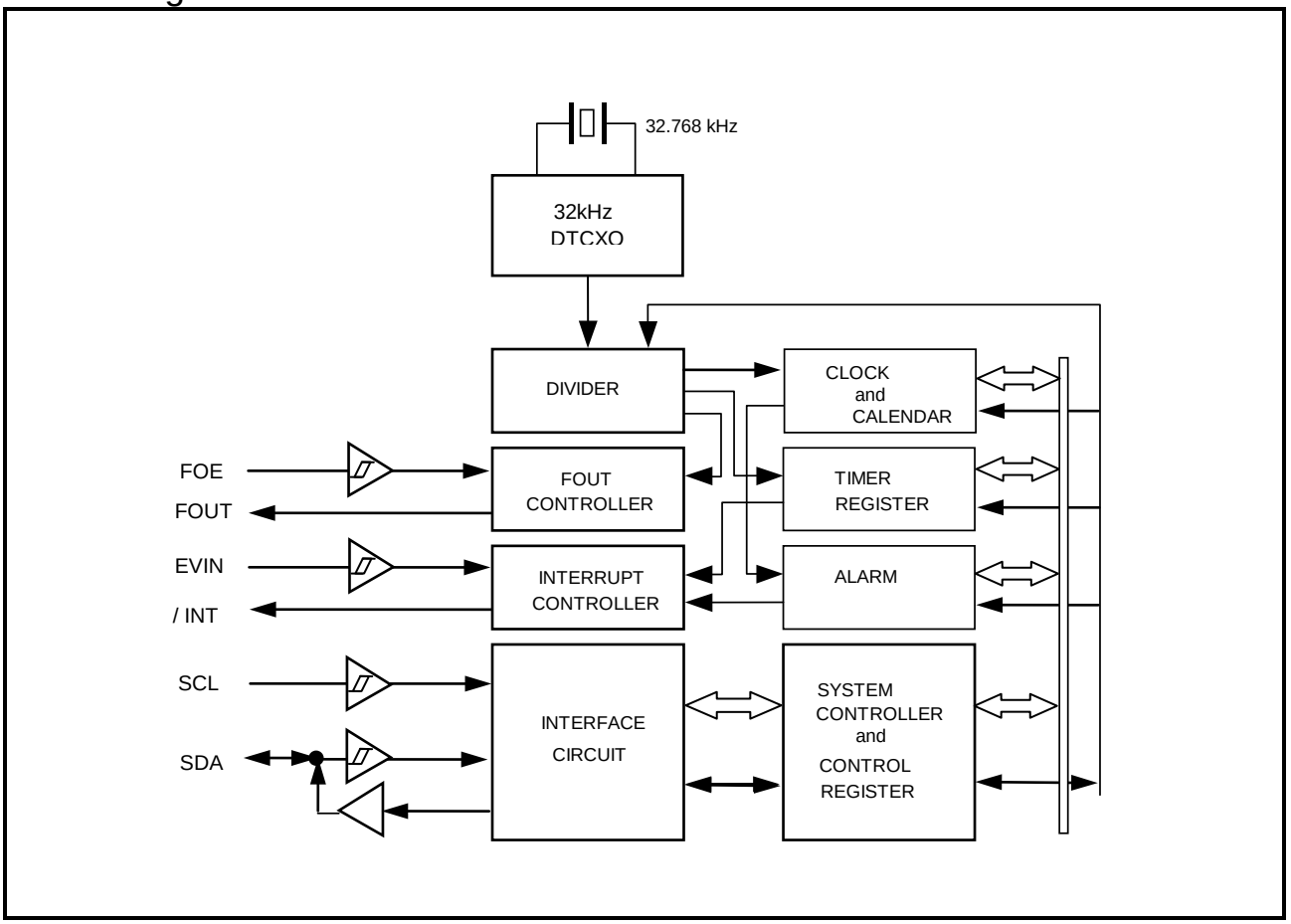
(*)Signal on pulse per second that synchronizes with Coordinated Universal Time output from GPS module

The I²C-BUS is a trademark of NXP Semiconductors.

## 1. Overview

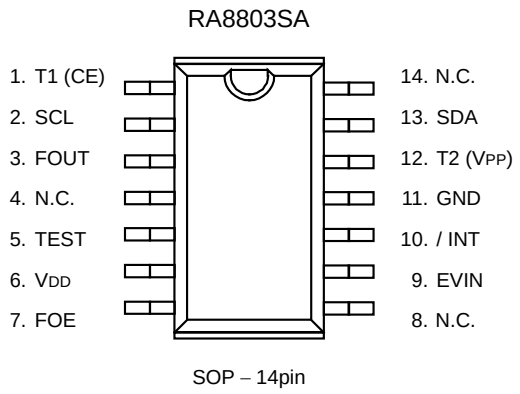
This module is an I²C bus interface-compliant real-time clock which includes a 32.768 kHz DTCXO. In addition to providing a calendar (year, month, date, day, hour, minute, second) function and a clock counter function, this module provides an abundance of other functions including an alarm function, fixed-cycle timer function, time update interrupt function, and 32.768 kHz output function.
The devices in this module are fabricated via a C-MOS process for low current consumption, which enables long-term battery back-up.
All of these many functions are implemented in SOP-14 pin package.

## 2. Block Diagram



# 3. Terminal description

## 3.1. Terminal connections




## 3.2. Pin Functions

| Signal name | I/O | Function |
|---|---|---|
| SDA | I/O | This pin's signal is used for input and output of address, data, and ACK bits, synchronized with the serial clock used for $I^2C$ communications.<br>Since the SDA pin is an N-ch open drain pin during output, be sure to connect a suitable pull-up resistance relative to the signal line capacity. |
| SCL | Input | This is the serial clock input pin for $I^2C$ Bus communications. |
| FOUT | Output | This is the C-MOS output pin with output control provided via the FOE pin.<br>When FOE = "H" (high level), this pin outputs a 32.768 kHz signal.<br>When output is stopped, the FOUT pin = "Hi-Z"( high impedance ). |
| FOE | Input | This is an input pin used to control the output mode of the FOUT pin.<br>When this pin's level is high, the FOUT pin is in output mode. When it is low, output via the FOUT pin is stopped. |
| / INT | Output | This pins is used to output alarm signals, timer signals, time update signals, and other signals. This pin is an open drain pin. |
| EVIN | Input | External event input pin. |
| VDD | – | This pin is connected to a positive power supply. |
| GND | – | This pin is connected to a ground. |
| TEST | Input | Use by the manufacture for testing. ( Do not connect externally.) |
| T1 (CE) | Input | Use by the manufacture for testing. ( Do not connect externally.) |
| T2 (VPP) | – | Use by the manufacture for testing. ( Do not connect externally.) |
| N.C. | – | This pin is not connected to the internal IC.<br>Leave N.C. pins open or connect them to GND or VDD. |

Note: Be sure to connect a bypass capacitor rated at least 0.1 µF between VDD and GND.

## 4. Absolute Maximum Ratings

GND = 0 V

| Item | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | Between $V_{DD}$ and GND | −0.3 to +6.5 | V |
| Input voltage (1) | $V_{IN1}$ | FOE pin | GND−0.3 to $V_{DD}$+0.3 | V |
| Input voltage (2) | $V_{IN2}$ | SCL and SDA pins | GND−0.3 to +6.5 | V |
| Output voltage (1) | $V_{OUT1}$ | FOUT pin | GND−0.3 to $V_{DD}$+0.3 | V |
| Output voltage (2) | $V_{OUT2}$ | SDA and /INT pins | GND−0.3 to +6.5 | V |
| Storage temperature | $T_{STG}$ | When stored separately, without packaging | −55 to +125 | °C |

## 5. Recommended Operating Conditions

GND = 0 V

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Operating supply voltage | $V_{DD}$ | Interface voltage | 1.6 | 3.0 | 5.5 | V |
| Temp. compensation voltage | $V_{TEM}$ | Temperature compensation voltage | 2.2 | 3.0 | 5.5 | V |
| Clock supply voltage | $V_{CLK}$ | − | 1.6 | 3.0 | 5.5 | V |
| Operating temperature | $T_{OPR}$ | No condensation | −40 | +25 | +85 | °C |

## 6. Frequency Characteristics

GND = 0 V

| Item | Symbol | Condition | | Rating | Unit |
|---|---|---|---|---|---|
| Frequency stability | $\Delta f / f$ | U A | Ta= 0 to +50 °C, $V_{DD}$=3.0 V<br>Ta=−40 to +85 °C, $V_{DD}$=3.0 V | ± 1.9 (*1)<br>± 3.4 (*2) | $\times 10^{-6}$ |
| | | U B | Ta= 0 to +50 °C, $V_{DD}$=3.0 V<br>Ta=−40 to +85 °C, $V_{DD}$=3.0 V | ± 3.8 (*3)<br>± 5.0 (*4) | |
| | | U C | Ta= 0 to +50 °C, $V_{DD}$=3.0 V<br>Ta=−30 to +70 °C, $V_{DD}$=3.0 V | ± 3.8 (*3)<br>± 5.0 (*4) | |
| | | A A | Ta= +25 °C, $V_{DD}$=3.0 V | +5± 5.0 (*5) | |
| Frequency/voltage characteristics | f / V | Ta= +25 °C, $V_{DD}$=2.2 V to 5.5 V | | ± 1.0 Max. | $\times 10^{-6}$ / V |
| Oscillation start time | $t_{STA}$ | Ta= +25 °C, $V_{DD}$=1.6 V<br>Ta=−40 to +85 °C, $V_{DD}$=1.6 V to 5.5 V | | 1.0 Max.<br>3.0 Max. | s |
| Aging | fa | Ta= +25 °C, $V_{DD}$=3.0 V, first year | | ± 3 Max. | $\times 10^{-6}$ / year |

*1) Equivalent to 5 seconds of month deviation. *2) Equivalent to 9 seconds of month deviation.
*3) Equivalent to 10 seconds of month deviation. *4) *5) Equivalent to 13 seconds of month deviation. ( excluding offset )

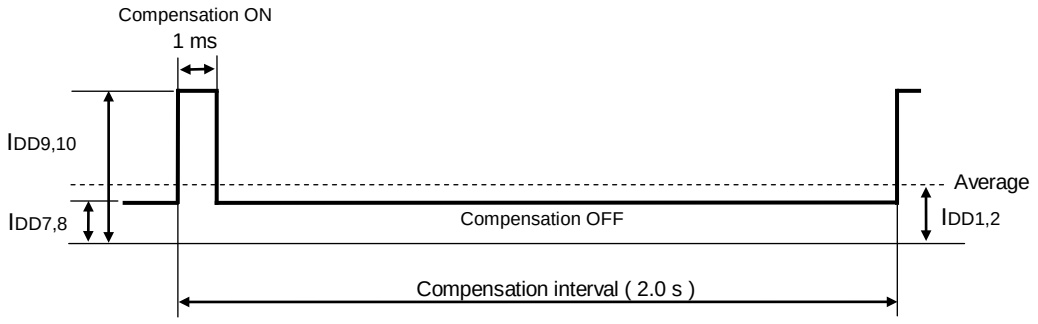
# 7. Electrical Characteristics

## 7.1. DC Characteristics

*Unless otherwise specified, GND = 0 V, $V_{DD}$ = 1.6 V to 5.5 V, Ta = −40 °C to +85 °C

| Item | Symbol | Condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Current consumption (1) | $I_{DD1}$ | $f_{SCL}$ = 0 Hz, / INT = $V_{DD}$<br>FOE = GND<br>FOUT : output OFF ( High Z )<br>Compensation interval 2.0 s | $V_{DD}$ = 5 V | | 0.75 | 3.4 | μA |
| Current consumption (2) | $I_{DD2}$ | | $V_{DD}$ = 3 V | | 0.75 | 2.1 | |
| Current consumption (3) | $I_{DD3}$ | $f_{SCL}$ = 0 Hz, / INT = $V_{DD}$<br>FOE = $V_{DD}$<br>FOUT :32.768 kHz, CL =0pF<br>Compensation interval 2.0 s | $V_{DD}$ = 5 V | | 2.0 | 7.5 | μA |
| Current consumption (4) | $I_{DD4}$ | | $V_{DD}$ = 3 V | | 1.5 | 5.0 | |
| Current consumption (5) | $I_{DD5}$ | $f_{SCL}$ = 0 Hz, / INT = $V_{DD}$<br>FOE = $V_{DD}$<br>FOUT :32.768 kHz, CL =30pF<br>Compensation interval 2.0 s | $V_{DD}$ = 5 V | | 7.0 | 20.0 | μA |
| Current consumption (6) | $I_{DD6}$ | | $V_{DD}$ = 3 V | | 4.5 | 12.0 | |
| Current consumption (7) | $I_{DD7}$ | $f_{SCL}$ = 0 Hz, / INT = $V_{DD}$<br>FOE = GND<br>FOUT : output OFF ( High Z )<br>Compensation OFF | $V_{DD}$ = 5 V | | 0.7 | 2.95 | μA |
| Current consumption (8) | $I_{DD8}$ | | $V_{DD}$ = 3 V | | 0.7 | 1.85 | |
| Current consumption (9) | $I_{DD9}$ | $f_{SCL}$ = 0 Hz, / INT = $V_{DD}$<br>FOE = GND<br>FOUT : output OFF ( High Z )<br>Compensation ON ( peak ) | $V_{DD}$ = 5 V | | 120 | 900 | μA |
| Current consumption (10) | $I_{DD10}$ | | $V_{DD}$ = 3 V | | 115 | 350 | |
| High-level input voltage | $V_{IH}$ | CE, DI, CLK, FOE, EVIN pins | | 0.8 × $V_{DD}$ | | 5.5 | V |
| Low-level input voltage | $V_{IL}$ | CE, DI, CLK, FOE, EVIN pins | | GND − 0.3 | | 0.2 × $V_{DD}$ | V |
| High-level output voltage | $V_{OH1}$ | FOUT pin | $V_{DD}$=5 V, $I_{OH}$=−1 mA | 4.5 | | 5.0 | V |
| | $V_{OH2}$ | | $V_{DD}$=3 V, $I_{OH}$=−1 mA | 2.2 | | 3.0 | |
| | $V_{OH3}$ | | $V_{DD}$=3 V, $I_{OH}$=−100 μA | 2.9 | | 3.0 | |
| Low-level output voltage | $V_{OL1}$ | FOUT pin | $V_{DD}$=5 V, $I_{OL}$=1 mA | GND | | GND+0.5 | V |
| | $V_{OL2}$ | | $V_{DD}$=3 V, $I_{OL}$=1 mA | GND | | GND+0.8 | |
| | $V_{OL3}$ | | $V_{DD}$=3 V, $I_{OL}$=100 μA | GND | | GND+0.1 | |
| | $V_{OL4}$ | / INT pin | $V_{DD}$=5 V, $I_{OL}$=1 mA | GND | | GND+0.25 | V |
| | $V_{OL5}$ | | $V_{DD}$=3 V, $I_{OL}$=1 mA | GND | | GND+0.4 | |
| | $V_{OL6}$ | SDA pin | $V_{DD}$ ≥2 V, $I_{OL}$=3 mA | GND | | GND+0.4 | V |
| Input leakage current | $I_{LK}$ | FOE, SCL, SDA pins , $V_{IN}$ = $V_{DD}$ or GND | | −0.5 | | 0.5 | μA |
| Output leakage current | $I_{OZ}$ | / INT, SDA, FOUT pins, $V_{OUT}$ = $V_{DD}$ or GND | | −0.5 | | 0.5 | μA |

- Temperature compensation and consumption current

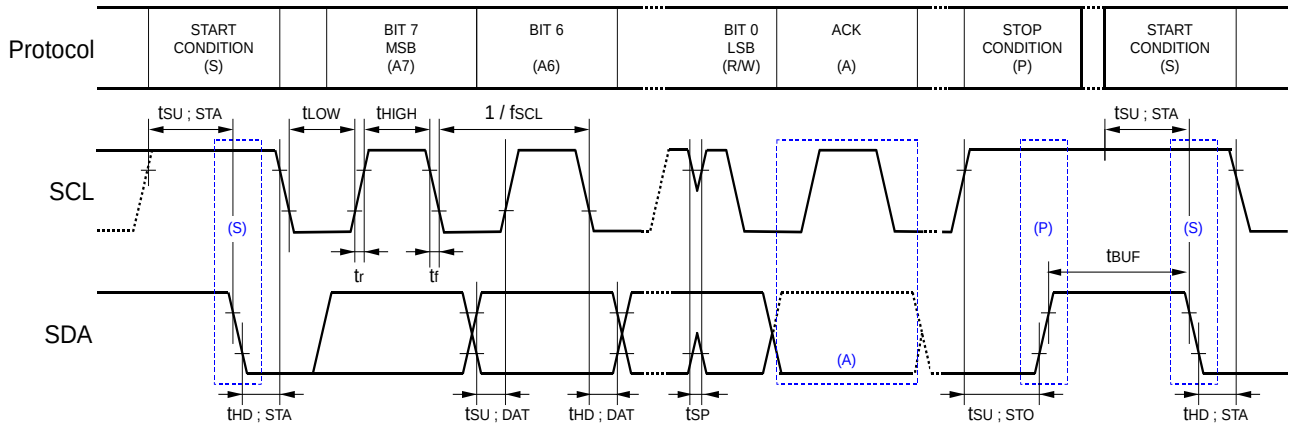


## 7.2. AC Characteristics

* Unless otherwise specified,
GND = 0 V , $V_{DD}$ = 1.8 V to 5.5 V , Ta = –40 °C to +85 °C

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| SCL clock frequency | $f_{SCL}$ | | | | 400 | kHz |
| Start condition setup time | $t_{SU;STA}$ | | 0.6 | | | µs |
| Start condition hold time | $t_{HD;STA}$ | | 0.6 | | | µs |
| Data setup time | $t_{SU;DAT}$ | | 100 | | | ns |
| Data hold time | $t_{HD;DAT}$ | | 0 | | 900 | ns |
| Stop condition setup time | $t_{SU;STO}$ | | 0.6 | | | µs |
| Bus idle time between start condition and stop condition | $t_{BUF}$ | | 1.3 | | | µs |
| Time when SCL = "L" | $t_{LOW}$ | | 1.3 | | | µs |
| Time when SCL = "H" | $t_{HIGH}$ | | 0.6 | | | µs |
| Rise time for SCL and SDA | $t_r$ | | | | 0.3 | µs |
| Fall time for SCL and SDA | $t_f$ | | | | 0.3 | µs |
| Allowable spike time on bus | $t_{SP}$ | | | | 50 | ns |
| FOUT duty | $t_W$ /t | 50% of $V_{DD}$ level | 40 | 50 | 60 | % |

Timing chart




Caution: When accessing this device, all communication from transmitting the start condition to transmitting the stop condition after access **should be completed within 0.95 seconds**.
If such communication requires **0.95 seconds** or longer, the $I^2C$ bus interface is reset by the internal bus timeout function.

# 8. Use Methods

## 8.1. Description of Registers

### 8.1.1. Write / Read and Bank Select

Address 00h to 0Fh : Basic time and calendar register
Address 10h to 1Fh : Extension register① … Adds 1/100s Counter.
Address 20h to 2Fh : Extension register② … Capture buffer and Event control registers.

### 8.1.2. Register table (Basic time and calendar register)

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Read | Write |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 00 | SEC | ○ | 40 | 20 | 10 | 8 | 4 | 2 | 1 | P | P |
| 01 | MIN | ○ | 40 | 20 | 10 | 8 | 4 | 2 | 1 | P | P |
| 02 | HOUR | ○ | ○ | 20 | 10 | 8 | 4 | 2 | 1 | P | P |
| 03 | WEEK | ○ | 6 | 5 | 4 | 3 | 2 | 1 | 0 | P | P |
| 04 | DAY | ○ | ○ | 20 | 10 | 8 | 4 | 2 | 1 | P | P |
| 05 | MONTH | ○ | ○ | ○ | 10 | 8 | 4 | 2 | 1 | P | P |
| 06 | YEAR | 80 | 40 | 20 | 10 | 8 | 4 | 2 | 1 | P | P |
| 07 | RAM | • | • | • | • | • | • | • | • | P | P |
| 08 | MIN Alarm | AE | 40 | 20 | 10 | 8 | 4 | 2 | 1 | P | P |
| 09 | HOUR Alarm | AE | • | 20 | 10 | 8 | 4 | 2 | 1 | P | P |
| 0A | WEEK Alarm | AE | 6 | 5 | 4 | 3 | 2 | 1 | 0 | P | P |
| | DAY Alarm | | • | 20 | 10 | 8 | 4 | 2 | 1 | | |
| 0B | Timer Counter 0 | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | P | P |
| 0C | Timer Counter 1 | • | • | • | • | 2048 | 1024 | 512 | 256 | P | P |
| 0D | Extension Register | TEST | WADA | USEL | TE | FSEL1 | FSEL0 | TSEL1 | TSEL0 | P | P |
| 0E | Flag Register | ○ | ○ | UF | TF | AF | EVF | VLF | VDET | P | P |
| 0F | Control Register | CSEL1 | CSEL0 | UIE | TIE | AIE | EIE | ○ | RESET | P | P |

P : Possible , I : Impossible

Note When after the initial power-up or when the result of read out the VLF bit is "1" , initialize all registers, before using the module.
Be sure to avoid entering incorrect date and time data, as clock operations are not guaranteed when the data or time data is incorrect.

∗1) During the initial power-up, the TEST bit is reset to "0" and the VLF bit is set to "1".
∗ At this point, all other register values are undefined, so be sure to perform a reset before using the module.

∗2) Only a "0" can be written to the UF, TF, AF, VLF, or VDET bit.

∗3) Any bit marked with "○" should be used with a value of "0" after initialization.

∗4) Any bit marked with "•" is a RAM bit that can be used to read or write any data.

∗5) The TEST bit is used by the manufacturer for testing. Be sure to set "0" for this bit when writing.

8.1.3. Register table (Extension register①)

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Read | Write |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 10 | 1/100 S | 80 | 40 | 20 | 10 | 8 | 4 | 2 | 1 | P | I |
| 11 | SEC | ○ | 40 | 20 | 10 | 8 | 4 | 2 | 1 | P | P |
| 12 | MIN | ○ | 40 | 20 | 10 | 8 | 4 | 2 | 1 | P | P |
| 13 | HOUR | ○ | ○ | 20 | 10 | 8 | 4 | 2 | 1 | P | P |
| 14 | WEEK | ○ | 6 | 5 | 4 | 3 | 2 | 1 | 0 | P | P |
| 15 | DAY | ○ | ○ | 20 | 10 | 8 | 4 | 2 | 1 | P | P |
| 16 | MONTH | ○ | ○ | ○ | 10 | 8 | 4 | 2 | 1 | P | P |
| 17 | YEAR | 80 | 40 | 20 | 10 | 8 | 4 | 2 | 1 | P | P |
| 18 | MIN Alarm | AE | 40 | 20 | 10 | 8 | 4 | 2 | 1 | P | P |
| 19 | HOUR Alarm | AE | • | 20 | 10 | 8 | 4 | 2 | 1 | P | P |
| 1A | WEEK Alarm | AE | 6 | 5 | 4 | 3 | 2 | 1 | 0 | P | P |
| | DAY Alarm | | • | 20 | 10 | 8 | 4 | 2 | 1 | | |
| 1B | Timer Counter 0 | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | P | P |
| 1C | Timer Counter 1 | • | • | • | • | 2048 | 1024 | 512 | 256 | P | P |
| 1D | Extension Register | TEST | WADA | USEL | TE | FSEL1 | FSEL0 | TSEL1 | TSEL0 | P | P |
| 1E | Flag Register | ○ | ○ | UF | TF | AF | EVF | VLF | VDET | P | P |
| 1F | Control Register | CSEL1 | CSEL0 | UIE | TIE | AIE | EIE | ○ | RESET | P | P |

1/100S Reg. is cleared to "00" by writing in the SEC Reg. or RESET bit and the ERST bit operation.

8.1.4. Register table (Extension register②)

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Read | Write |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 20 | 1/100 S CP | 80 | 40 | 20 | 10 | 8 | 4 | 2 | 1 | P | I |
| 21 | SEC CP | ○ | 40 | 20 | 10 | 8 | 4 | 2 | 1 | P | I |
| 22 | – | – | – | – | – | – | – | – | – | – | – |
| 23 | – | – | – | – | – | – | – | – | – | – | – |
| 24 | – | – | – | – | – | – | – | – | – | – | – |
| 25 | – | – | – | – | – | – | – | – | – | – | – |
| 26 | – | – | – | – | – | – | – | – | – | – | – |
| 27 | – | – | – | – | – | – | – | – | – | – | – |
| 28 | – | – | – | – | – | – | – | – | – | – | – |
| 29 | – | – | – | – | – | – | – | – | – | – | – |
| 2A | – | – | – | – | – | – | – | – | – | – | – |
| 2B | – | – | – | – | – | – | – | – | – | – | – |
| 2C | OSC Offset | ○ | ○ | ○ | ○ | OFS3 | OFS2 | OFS1 | OFS0 | P | P |
| 2D | – | – | – | – | – | – | – | – | – | – | – |
| 2E | – | – | – | – | – | – | – | – | – | – | – |
| 2F | Event Control | ECP | EHL | ET1 | ET0 | ○ | ○ | ○ | ERST | P | P |

When an initial power on, frequency offset is ±0 selected by "0000".

## 8.2. Details of Registers

### 8.2.1. Clock counter ( 1/100S, SEC - HOUR )

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 10 | 1/100 S | 80 | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| 00, 11 | SEC | ○ | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| 01, 12 | MIN | ○ | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| 02, 13 | HOUR | ○ | ○ | 20 | 10 | 8 | 4 | 2 | 1 |

*) "o" indicates write-protected bits. A zero is always read from these bits.

- The clock counter counts 1/100s, seconds, minutes, and hours.
- The data format is BCD format. For example, when the "seconds" register value is "0101 1001" it indicates 59 seconds.

* Note with caution that writing non-existent time data may interfere with normal operation of the clock counter.

1) 1/100 Second counter

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 10 | 1/100 S | 80 | 40 | 20 | 10 | 8 | 4 | 2 | 1 |

- This second counter counts from "00" to "01," "02," and up to 99/100 seconds, after which it starts again from 00 seconds.

2) Second counter

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 00, 11 | SEC | ○ | 40 | 20 | 10 | 8 | 4 | 2 | 1 |

- This second counter counts from "00" to "01," "02," and up to 59 seconds, after which it starts again from 00 seconds.

3) Minute counter

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 01, 12 | MIN | ○ | 40 | 20 | 10 | 8 | 4 | 2 | 1 |

- This minute counter counts from "00" to "01," "02," and up to 59 minutes, after which it starts again from 00 minutes.

4) Hour counter

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 02, 13 | HOUR | ○ | ○ | 20 | 10 | 8 | 4 | 2 | 1 |

- This hour counter counts from "00" hours to "01," "02," and up to 23 hours, after which it starts again from 00 hours.

8.2.2. Calendar counter ( WEEK - YEAR )

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 03, 14 | WEEK | ○ | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

*) "o" indicates write-protected bits. A zero is always read from these bits.

1) Day of the WEEK counter

- The day (of the week) is indicated by 7 bits, bit 0 to bit 6.
  The day data values are counted as: Day 01h → Day 02h → Day 04h → Day 08h → Day 10h → Day 20h → Day 40h → Day 01h → Day 02h, etc.
- The correspondence between days and count values is shown below.

| WEEK | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Day | Data [h] |
|---|---|---|---|---|---|---|---|---|---|---|
| Write/Read | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **1** | Sunday | 01 h |
| | 0 | 0 | 0 | 0 | 0 | 0 | **1** | 0 | Monday | 02 h |
| | 0 | 0 | 0 | 0 | 0 | **1** | 0 | 0 | Tuesday | 04 h |
| | 0 | 0 | 0 | 0 | **1** | 0 | 0 | 0 | Wednesday | 08 h |
| | 0 | 0 | 0 | **1** | 0 | 0 | 0 | 0 | Thursday | 10 h |
| | 0 | 0 | **1** | 0 | 0 | 0 | 0 | 0 | Friday | 20 h |
| | 0 | **1** | 0 | 0 | 0 | 0 | 0 | 0 | Saturday | 40 h |
| Write prohibit | * Do not set "1" to more than one day at the same time. Also, note with caution that any setting other than the seven shown above should not be made as it may interfere with normal operation. | | | | | | | | – | – |

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 04, 15 | DAY | ○ | ○ | 20 | 10 | 8 | 4 | 2 | 1 |
| 05, 16 | MONTH | ○ | ○ | ○ | 10 | 8 | 4 | 2 | 1 |
| 06, 17 | YEAR | 80 | 40 | 20 | 10 | 8 | 4 | 2 | 1 |

*) "o" indicates write-protected bits. A zero is always read from these bits.

- The auto calendar function updates all dates, months, and years from January 1, 2001 to December 31, 2099.
- The data format is BCD format. For example, a date register value of "0011 0001" indicates the 31st.

* Note with caution that writing non-existent date data may interfere with normal operation of the calendar counter.

2) Date counter

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 04, 15 | DAY | ○ | ○ | 20 | 10 | 8 | 4 | 2 | 1 |

- The updating of dates by the date counter varies according to the month setting.

* A leap year is set whenever the year value is a multiple of four (such as 04, 08, 12, 88, 92, or 96). In February of a leap year, the counter counts dates from "01," "02," "03," to "28," "29," "01," etc.

| DAY | Month | Date update pattern |
|---|---|---|
| Write/Read | 1, 3, 5, 7, 8, 10, or 12 | 01, 02, 03 ~ 30, 31, 01 ~ |
| | 4, 6, 9, or 11 | 01, 02, 03 ~ 30, 01, 02 ~ |
| | February in normal year | 01, 02, 03 ~ 28, 01, 02 ~ |
| | February in leap year | 01, 02, 03 ~ 28, 29, 01 ~ |

3) Month counter

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 05, 16 | MONTH | ○ | ○ | ○ | 10 | 8 | 4 | 2 | 1 |

- The month counter counts from 01 (January), 02 (February), and up to 12 (December), then starts again at 01 (January).

4) Year counter

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 06, 17 | YEAR | Y80 | Y40 | Y20 | Y10 | Y8 | Y4 | Y2 | Y1 |

- The year counter counts from 00, 01, 02 and up to 99, then starts again at 00.
- Any year that is a multiple of four (04, 08, 12, 88, 92, 96, etc.) is handled as a leap year.

8.2.3. Alarm registers

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 08, 18 | MIN Alarm | AE | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| 09, 19 | HOUR Alarm | AE | • | 20 | 10 | 8 | 4 | 2 | 1 |
| 0A, 1A | WEEK Alarm | AE | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | DAY Alarm | | • | 20 | 10 | 8 | 4 | 2 | 1 |

- The alarm interrupt function is used, along with the AEI, AF, and WADA bits, to set alarms for specified date, day, hour, and minute values.
- When the settings in the above alarm registers and the WADA bit match the current time, the /INT pin goes to low level and "1" is set to the AF bit to report that and alarm interrupt event has occurred.

8.2.4. Fixed-cycle timer control registers

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0B, 1B | Timer Counter 0 | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
| 0C, 1C | Timer Counter 1 | • | • | • | • | 2048 | 1024 | 512 | 256 |

- These registers are used to set the preset countdown value for the fixed-cycle timer interrupt function. The TE, TF, TIE, and TSEL0/1 bits are also used to set the fixed-cycle timer interrupt function.
- When the value in the above fixed-cycle timer control register changes from 001h to 000h, the /INT pin goes to low level and "1" is set to the TF bit to report that a fixed-cycle timer interrupt event has occurred.

8.2.5. Extension register

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0D, 1D | Extension Register (Default) | TEST (0) | WADA (–) | USEL (–) | TE (–) | FSEL1 (0) | FSEL0 (0) | TSEL1 (–) | TSEL0 (–) |

∗1) The default value is the value that is read (or is set internally) after powering up from 0 V.

∗2) "o" indicates write-protected bits. A zero is always read from these bits.

∗3) "–" indicates a default value is undefined.

- This register is used to specify the target for the alarm function or time update interrupt function and to select or set operations such as fixed-cycle timer operations.

1) TEST bit

This is the manufacturer's test bit. Its value should always be "0".
Be careful to avoid writing a "1" to this bit when writing to other bits.

| **TEST** | Data | Description |
|---|---|---|
| Write/Read | 0 | Normal operation mode ∗ Default |
| | 1 | Setting prohibited (manufacturer's test bit) |

2) WADA ( Week Alarm/Day Alarm ) bit

This bit is used to specify either WEEK or DAY as the target of the alarm interrupt function.
Writing a "1" to this bit specifies DAY as the comparison obLCct for the alarm interrupt function.
Writing a "0" to this bit specifies WEEK as the comparison obLCct for the alarm interrupt function.

3) USEL ( Update Interrupt Select ) bit

This bit is used to specify either "second update" or "minute update" as the update generation timing of the time update interrupt function.

| **USEL** | Data | update interrupts | Auto reset time $t_{RTN}$ |
|---|---|---|---|
| Write/Read | 0 | second update ∗ Default | 500 ms |
| | 1 | minute update | 7.813 ms |

4) TE ( Timer Enable ) bit

This bit controls the start/stop setting for the fixed-cycle timer interrupt function.
Writing a "1" to this bit specifies starting of the fixed-cycle timer interrupt function (a countdown starts from a preset value).
Writing a "0" to this bit specifies stopping of the fixed-cycle timer interrupt function.

5) FSEL0,1 ( FOUT frequency Select 0, 1 ) bits
The combination of these two bits is used to set the FOUT frequency.

| **FSEL0,1** | FSEL1 (bit 3) | FSEL0 (bit 2) | FOUT frequency |
|---|---|---|---|
| Write/Read | 0 | 0 | 32768 Hz Output ∗ Default |
| | 0 | 1 | 1024 Hz Output |
| | 1 | 0 | 1 Hz Output |
| | 1 | 1 | 32768 Hz Output |

6) TSEL0,1 ( Timer Select 0, 1 ) bits
The combination of these two bits is used to set the countdown period (source clock) for the fixed-cycle timer interrupt function (four settings can be made).

| **TSEL0,1** | TSEL1 (bit 1) | TSEL0 (bit 0) | Source clock |
|---|---|---|---|
| Write/Read | 0 | 0 | 4096 Hz / Once per 244.14 μs |
| | 0 | 1 | 64 Hz / Once per 15.625 ms |
| | 1 | 0 | "Second" update / Once per second |
| | 1 | 1 | "Minute" update / Once per minute |

8.2.6. Flag register

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0E, 1E | Flag register (Default) | ○ (0) | ○ (0) | UF (–) | TF (–) | AF (–) | EVF (–) | VLF (1) | VDET (1) |

∗1) The default value is the value that is read (or is set internally) after powering up from 0 V.
∗2) "o" indicates write-protected bits. A zero is always read from these bits.
∗3) "–" indicates a default value is undefined.

- This register is used to detect the occurrence of various interrupt events and reliability problems in internal data.

1) UF ( Update Flag ) bit
If set to "0" beforehand, this flag bit's value changes from "0" to 1" when a time update interrupt event has occurred. Once this flag bit's value is "1", its value is retained until a "0" is written to it.
∗ For details, see "8.4. Time Update Interrupt Function".

2) TF ( Timer Flag ) bit
If set to "0" beforehand, this flag bit's value changes from "0" to 1" when a fixed-cycle timer interrupt event has occurred. Once this flag bit's value is "1", its value is retained until a "0" is written to it.
∗ For details, see "8.3. Fixed-cycle Timer Interrupt Function".

3) AF ( Alarm Flag ) bit
If set to "0" beforehand, this flag bit's value changes from "0" to 1" when an alarm interrupt event has occurred. Once this flag bit's value is "1", its value is retained until a "0" is written to it.
∗ For details, see "8.5. Alarm Interrupt Function".

4) EVF ( Event Flag ) bit
If set to "0" beforehand, this flag bit's value changes from "0" to 1" when a event input interrupt has occurred. Once this flag bit's value is "1", its value is retained until a "0" is written to it.

5) VLF ( Voltage Low Flag ) bit
This flag bit indicates the retained status of clock operations or internal data. Its value changes from "0" to "1" when data loss occurs, such as due to a supply voltage drop. Once this flag bit's value is "1", its value is retained until a "0" is written to it.
When after powering up from 0 V this bit's value is "1" .

| VLF | Data | Description |
|---|---|---|
| Write | 0 | The VLF bit is cleared to zero to prepare for the next status detection. |
| | 1 | This bit is invalid after a "1" has been written to it. |
| Read | 0 | Data loss is not detected. |
| | 1 | Data loss is detected. All registers must be initialized.<br>( This setting is retained until a "zero" is written to this bit. ) |

5) VDET ( Voltage Detection Flag ) bit

This flag bit indicates the status of temperature compensation. Its value changes from "0" to "1" when stop the temperature compensation, such as due to a supply voltage drop. Once this flag bit's value is "1", its value is retained until a "0" is written to it.

When after powering up from 0 V this bit's value is "1".

| VDET | Data | Description |
|---|---|---|
| Write | 0 | The VDET bit is cleared to zero to prepare for the next low voltage detection. |
| | 1 | The write access of "1" to this bit is invalid. |
| Read | 0 | Temperature compensation is normal. |
| | 1 | Temperature compensation is stop detected. |

8.2.7. Control register

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0F, 1F | Control Register<br>(Default) | CSEL1<br>(0) | CSEL0<br>(1) | UIE<br>(–) | TIE<br>(–) | AIE<br>(–) | EIE<br>(–) | ○<br>(0) | RESET<br>(–) |

∗1) The default value is the value that is read (or is set internally) after powering up from 0 V.

∗2) "o" indicates write-protected bits. A zero is always read from these bits.

∗3) "–" indicates no default value has been defined.

- This register is used to control interrupt event output from the /INT pin and the stop/start status of clock and calendar operations.

1) CSEL0,1 ( Compensation interval Select 0, 1 ) bits

The combination of these two bits is used to set the temperature compensation interval.

| CSEL0,1 | CSEL1 (bit 7) | CSEL0 (bit 6) | Compensation interval | |
|---|---|---|---|---|
| Write/Read | 0 | 0 | 0.5 s | |
| | 0 | 1 | 2.0 s | ∗ Default |
| | 1 | 0 | 10 s | |
| | 1 | 1 | 30 s | |

2) UIE ( Update Interrupt Enable ) bit

When a time update interrupt event is generated (when the UF bit value changes from "0" to "1"), this bit's value specifies if an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status remains Hi-Z).

When a "1" is written to this bit, an interrupt signal is generated (/INT status changes from Hi-Z to low) when an interrupt event is generated.

When a "0" is written to this bit, no interrupt signal is generated when an interrupt event occurs.

| UIE | Data | Function |
|---|---|---|
| Write/Read | 0 | When a time update interrupt event occurs, an interrupt signal is not generated or is canceled (/INT status changes from low to Hi-Z). |
| | 1 | When a time update interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low).<br>* When a time update interrupt event occurs, low-level output from the /INT pin occurs only when the value of the control register's UIE bit is "1". This /INT status is automatically cleared (/INT status changes from low to Hi-Z) 7.8 ms after the interrupt occurs. |

2) TIE ( Timer Interrupt Enable ) bit

When a fixed-cycle timer interrupt event occurs (when the TF bit value changes from "0" to "1"), this bit's value specifies if an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status remains Hi-Z).

When a "1" is written to this bit, an interrupt signal is generated (/INT status changes from Hi-Z to low) when an interrupt event is generated.

When a "0" is written to this bit, no interrupt signal is generated when an interrupt event occurs.

| TIE | Data | Function |
|---|---|---|
| Write/Read | 0 | When a fixed-cycle timer interrupt event occurs, an interrupt signal is not generated or is canceled (/INT status changes from low to Hi-Z). |
| | 1 | When a fixed-cycle timer interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low).<br>* When a fixed-cycle timer interrupt event has been generated low-level output from the /INT pin occurs only when the value of the control register's TIE bit is "1". Up to 7.8 ms after the interrupt occurs, the /INT status is automatically cleared (/INT status changes from low to Hi-Z). |

3) AIE ( Alarm Interrupt Enable ) bit

When an alarm timer interrupt event occurs (when the AF bit value changes from "0" to "1"), this bit's value specifies if an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status remains Hi-Z).

When a "1" is written to this bit, an interrupt signal is generated (/INT status changes from Hi-Z to low) when an interrupt event is generated.

When a "0" is written to this bit, no interrupt signal is generated when an interrupt event occurs.

| AIE | Data | Function |
|---|---|---|
| Write/Read | 0 | When an alarm interrupt event occurs, an interrupt signal is not generated or is canceled (/INT status changes from low to Hi-Z). |
| | 1 | When an alarm interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low).<br>* When an alarm interrupt event has been generated low-level output from the /INT pin occurs only when the value of the control register's AIE bit is "1". This setting is retained until the AF bit value is cleared to zero. (No automatic cancellation) |

* For details, see "8.5. Alarm Interrupt Function".

**[Caution]**

(1) The /INT pin is a shared interrupt output pin for three types of interrupts. It outputs the OR'ed result of these interrupt outputs. When an interrupt has occurred (when the /INT pin is at low level), the UF, TF, read AF flags to determine which flag has a value of "1" (this indicates which type of interrupt event has occurred).

(2) To keep the /INT pin from changing to low level, write "0" to the UIE, TIE, and AIE bits. To check whether an event has occurred without outputting any interrupts via the /INT pin, use software to monitor the value of the UF, TF, and AF interrupt flags.

4) EIE ( Event Interrupt Enable ) bit

When a Event input is generated (when the EVF bit value changes from "0" to "1"), this bit's value specifies if an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status remains Hi-Z). When a "1" is written to this bit, an interrupt signal is generated (/INT status changes from Hi-Z to low) when an interrupt event is generated.

When a "0" is written to this bit, no interrupt signal is generated when an interrupt event occurs.

5) RESET bit

When this bit is set to "1", values (less than seconds) of the counter in the Clock & Calendar circuitry is reset, and the clock also stops.

After "1" is written to this bit, this can be released by setting CE to "L".

8.2.8. OSC Offset Contorol

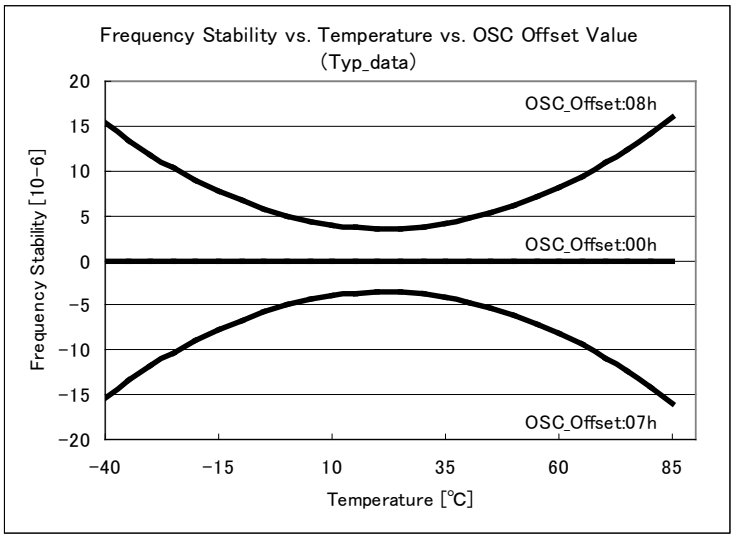
| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 2C | OSC Offset | ○ | ○ | ○ | ○ | OFS3 | OFS2 | OFS1 | OFS0 |

1) OFS bits (OFS3-OFS0)

The offset adjustment is done to the oscillation frequency.

| OFS3 | OFS2 | OFS1 | OFS0 | Adjust value ( x $10^{-6}$ ) RA8803SA |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | ± 0.0 |
| 0 | 0 | 0 | 1 | −0.6 |
| 0 | 0 | 1 | 0 | −1.2 |
| 0 | 0 | 1 | 1 | −1.8 |
| 0 | 1 | 0 | 0 | −2.4 |
| 0 | 1 | 0 | 1 | −3.0 |
| 0 | 1 | 1 | 0 | −3.6 |
| 0 | 1 | 1 | 1 | −4.2 |
| 1 | 0 | 0 | 0 | +4.8 |
| 1 | 0 | 0 | 1 | +4.2 |
| 1 | 0 | 1 | 0 | +3.6 |
| 1 | 0 | 1 | 1 | +3.0 |
| 1 | 1 | 0 | 0 | +2.4 |
| 1 | 1 | 0 | 1 | +1.8 |
| 1 | 1 | 1 | 0 | +1.2 |
| 1 | 1 | 1 | 1 | +0.6 |

*The OFS register affects the frequency stability. Please refer to a lower graph.
Please be careful if you offset and adjust it.
The offset function is effective for frequency adjustment at the normal temperature.



8.2.9. Capture Buffer / Event control

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 20 | 1/100 S CP | 80 | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| 21 | SEC CP | ○ | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| 2F | Event Control | ECP | EHL | ET1 | ET0 | ○ | ○ | ○ | ERST |

It is a register that sets it concerning the event detection.

1) ECP bit ( Event Capture enable )

It is specified whether to do the second and 1/100S data to the capture buffer in capture when the event is detected.

| ECP | Operation |
|---|---|
| 0 | Capture doesn't operate |
| 1 | Capture operation |

2) EHL bit ( High/Low detection select )

The disregard level of the event input is specified.
The event is detected by maintaining the level specified by the EHL bit longer than the chattering removal cycle.

| EHL | Operation |
|---|---|
| 0 | "L" level detect |
| 1 | "H" level detect |

3) ET1, ET0 bits ( Event chattering Time Set )

The removal cycle of the chattering removal function is set.

・Chattering removal cycle

| ET1 | ET0 | Cycle |
|---|---|---|
| 0 | 0 | not provided |
| 0 | 1 | 3.9 ms |
| 1 | 0 | 15.6 ms |
| 1 | 1 | 125 ms |

4) ERST bit

When this bit is made "1", the counter of the Clock & Calendar circuit (counter for 16kHz to 2Hz and 1/100 seconds) at less than second is reset synchronizing with the external event detection.

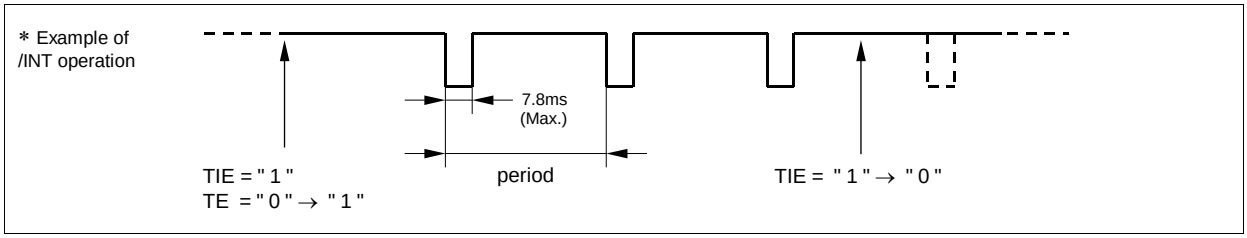
ALL "0" is cleared to CP and the CP register of the second at the same time for 1/100 seconds.

Timing continues until the event is generated after "1" is written in the ERST bit.
The counter at less than second when an external event is detected is reset, and the ERST bit is cleared.
Moreover, it is also possible to assume this reset action to be invalid by doing "0" writing directly to the ERST bit before the event is generated.

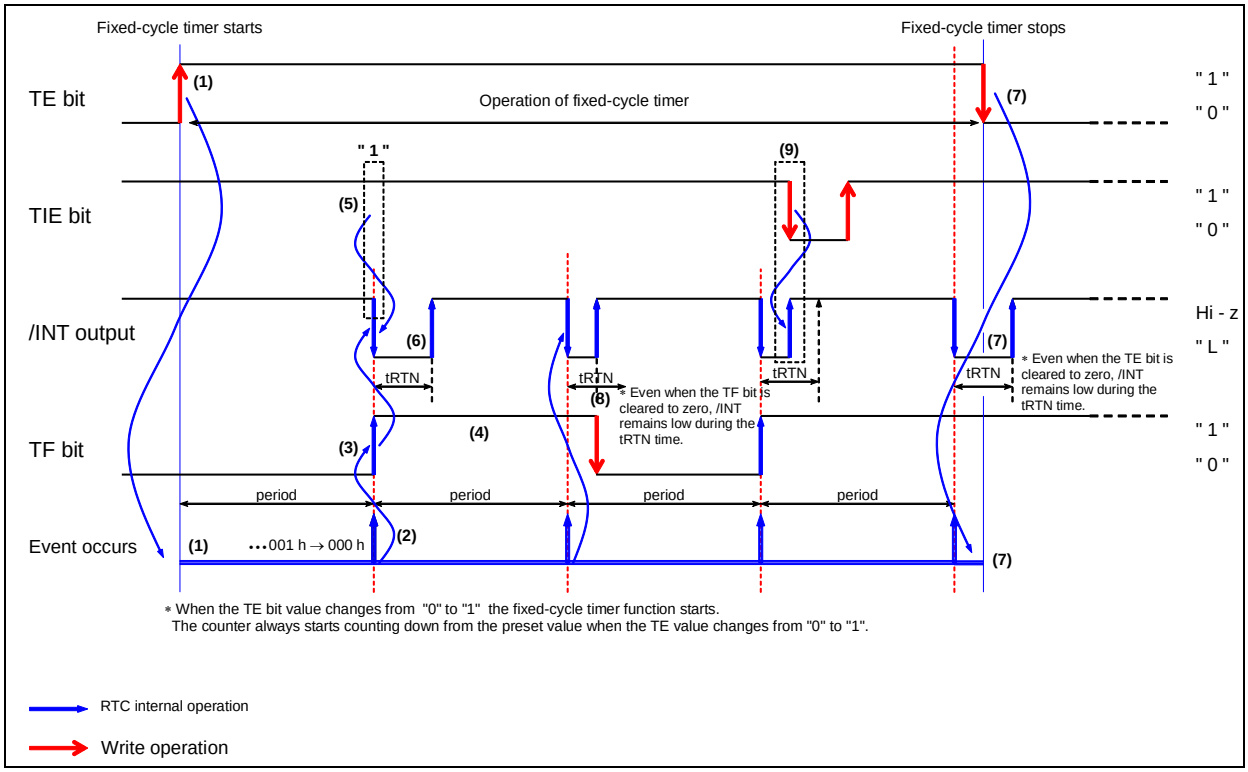
When the highly accurate time suiting is done, this bit is used.
The time for the counter at less than second to be reset influences the operation of the alarm, the fixed cycle timer, and the update interrupt of time, etc.

## 8.3. Fixed-cycle Timer Interrupt Function

The fixed-cycle timer interrupt generation function generates an interrupt event periodically at any fixed cycle set between 244.14 μs and 4095 minutes.
When an interrupt event is generated, the /INT pin goes to low level and "1" is set to the TF bit to report that an event has occurred. (However, when a fixed-cycle timer interrupt event has been generated low-level output from the /INT pin occurs only when the value of the control register's TIE bit is "1". Up to 7.8 ms after the interrupt occurs, the /INT status is automatically cleared (/INT status changes from low-level to Hi-Z).




### 8.3.1. Diagram of fixed-cycle timer interrupt function




(1) When a "1" is written to the TE bit, the fixed-cycle timer countdown starts from the preset value.

(2) A fixed-cycle timer interrupt event starts a countdown based on the countdown period (source clock). When the count value changes from 001h to 000h, an interrupt event occurs.
∗ After the interrupt event that occurs when the count value changes from 001h to 000h, the counter automatically reloads the preset value and again starts to count down. (Repeated operation)

(3) When a fixed-cycle timer interrupt event occurs, "1" is written to the TF bit.

(4) When the TF bit = "1" its value is retained until it is cleared to zero.

(5) If the TIE bit = "1" when a fixed-cycle timer interrupt occurs, /INT pin output goes low.
∗ If the TIE bit = "0" when a fixed-cycle timer interrupt occurs, /INT pin output remains Hi-Z.

(6) Output from the /INT pin remains low during the tRTN period following each event, after which it is automatically cleared to Hi-Z status.
∗ /INT is again set low when the next interrupt event occurs.

(7) When a "0" is written to the TE bit, the fixed-cycle timer function is stopped and the /INT pin is set to Hi-Z status.
∗ When /INT = low, the fixed-cycle timer function is stopped. The tRTN period is the maximum amount of time before the /INT pin status changes from low to Hi-Z.

(8) When /INT = low, the /INT pin status changes from low to Hi-Z as soon as the TF bit value changes from "1" to "0".

(9) When /INT = low, the /INT pin status changes from low to Hi-Z as soon as the TIE bit value changes from "1" to "0".

8.3.2. Related registers for function of time update interrupts.

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0B, 1B | Timer Counter 0 | **128** | **64** | **32** | **16** | **8** | **4** | **2** | **1** |
| 0C, 1C | Timer Counter 1 | • | • | • | • | **2048** | **1024** | **512** | **256** |
| 0D, 1D | Extension Register | TEST | WADA | USEL | **TE** | FSEL1 | FSEL0 | **TSEL1** | **TSEL0** |
| 0E, 1E | Flag Register | ○ | ○ | UF | **TF** | AF | EVF | VLF | VDET |
| 0F, 1F | Control Register | CSEL1 | CSEL0 | UIE | **TIE** | AIE | EIE | ○ | RESET |

∗1) "o" indicates write-protected bits. A zero is always read from these bits.

∗2) Bits marked with "•" are RAM bits that can contain any value and are read/write-accessible.

∗ Before entering settings for operations, we recommend writing a "0" to the TE and TIE bits to prevent hardware interrupts from occurring inadvertently while entering settings.

∗ When the STOP bit or RESET bit value is "1" the time update interrupt function operates only partially. (Operation continues if the source clock setting is 4096 Hz. Otherwise, operation is stopped.)

∗ When the fixed-cycle timer interrupt function is not being used, the fixed-cycle timer control register (Reg – B to C) can be used as a RAM register. In such cases, stop the fixed-cycle timer function by writing "0" to the TE and TIE bits.

1) TSEL0,1 bits (Timer Select 0, 1)

The combination of these two bits is used to set the countdown period (source clock) for the fixed-cycle timer interrupt function (four settings can be made).

| TSEL0,1 | TSEL1 (bit 1) | TSEL0 (bit 0) | Source clock | Auto reset time tRTN | Effects of RESET bits |
|---|---|---|---|---|---|
| Write/Read | 0 | 0 | 4096 Hz /Once per 244.14 μs | 122 μs | – |
| | 0 | 1 | 64 Hz / Once per 15.625 ms | 7.8125 ms | ∗ Does not operate when the RESET bit value is "1". |
| | 1 | 0 | "Second" update /Once per second | 7.8125 ms | |
| | 1 | 1 | "Minute" update /Once per minute | 7.8125 ms | |

∗1) The /INT pin's auto reset time (tRTN) varies as shown above according to the source clock setting.

∗2) When the source clock has been set to "second update" or "minute update", the timing of both countdown and interrupts is coordinated with the clock update timing.

2) Fixed-cycle Timer Control register (Reg - B to C)

This register is used to set the default (preset) value for the counter. Any count value from 1 (001 h) to 4095 (FFFh) can be set. The counter counts down based on the source clock's period, and when the count value changes from 001h to 000h, the TF bit value becomes "1".

The countdown that starts when the TE bit value changes from "0" to "1" always begins from the preset value. Be sure to write "0" to the TE bit before writing the preset value. If a value is written while TE = "1" the first subsequent event will not be generated correctly.

| Address C Timer Counter 1 | | | | | | | | Address B Timer Counter 0 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| • | • | • | • | 2048 | 1024 | 512 | 256 | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |

3) TE (Timer Enable) bit

This bit controls the start/stop setting for the fixed-cycle timer interrupt function.

| **TE** | Data | Description |
|---|---|---|
| Write/Read | 0 | Stops fixed-cycle timer interrupt function. |
| | 1 | Starts fixed-cycle timer interrupt function.<br>∗ The countdown that starts when the TE bit value changes from "0" to "1" always begins from the preset value. |

4) TF (Timer Flag) bit

If set to "0" beforehand, this flag bit's value changes from "0" to 1" when a fixed-cycle timer interrupt event has occurred. Once this flag bit's value is "1", its value is retained until a "0" is written to it.

| **TF** | Data | Description |
|---|---|---|
| Write | 0 | The TF bit is cleared to zero to prepare for the next status detection<br>∗ Clearing this bit to zero does not enable the /INT low output status to be cleared (to Hi-Z). |
| | 1 | This bit is invalid after a "1" has been written to it. |
| Read | 0 | Fixed-cycle timer interrupt events are not detected. |
| | 1 | Fixed-cycle timer interrupt events are detected.<br>(Result is retained until this bit is cleared to zero.) |

5) TIE (Timer Interrupt Enable) bit
When a fixed-cycle timer interrupt event occurs (when the TF bit value changes from "0" to "1"), this bit's value specifies whether an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status remains Hi-Z).

| **TIE** | Data | Description |
|---|---|---|
| Write/Read | 0 | 1) When a fixed-cycle timer interrupt event occurs, an interrupt signal is not generated or is canceled (/INT status remains Hi-Z).<br>2) When a fixed-cycle timer interrupt event occurs, the interrupt signal is canceled (/INT status changes from low to Hi-Z).<br>* Even when the TIE bit value is "0" another interrupt event may change the /INT status to low (or may hold /INT = "L"). |
| | 1 | When a fixed-cycle timer interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low).<br>* When a fixed-cycle timer interrupt event has been generated low-level output from the /INT pin occurs only when the value of the control register's TIE bit is "1". Up to 7.8 ms after the interrupt occurs, the /INT status is automatically cleared (/INT status changes from low to Hi-Z). |

8.3.3. Fixed-cycle timer interrupt interval (example)

| Timer Counter setting | Source clock | | | |
|---|---|---|---|---|
| | 4096 Hz TSEL1,0 = 0,0 | 64 Hz TSEL1,0 = 0,1 | "Second" update TSEL1,0 = 1,0 | "Minute" update TSEL1,0 = 1,1 |
| 0 | – | – | – | – |
| 1 | 244.14 μs | 15.625 ms | 1 s | 1 min |
| 2 | 488.28 μs | 31.25 ms | 2 s | 2 min |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |
| 41 | 10.010 ms | 640.63 ms | 41 s | 41 min |
| 205 | 50.049 ms | 3.203 s | 205 s | 205 min |
| 410 | 100.10 ms | 6.406 s | 410 s | 410 min |
| 2048 | 500.00 ms | 32.000 s | 2048 s | 2048 min |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |
| 4095 | 0.9998 s | 63.984 s | 4095 s | 4095 min |

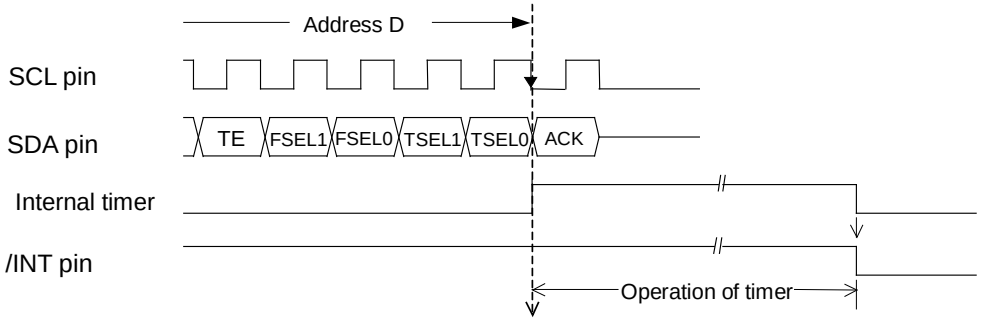
- Time error in fixed-cycle timer
  A time error in the fixed-cycle timer will produce a positive or negative time period error in the selected source clock. The fixed-cycle timer's time is within the following range relative to the time setting.

(Fixed-cycle timer's time setting (*) – source clock period) to (timer's time setting)
*) The timer's time setting = source clock period × timer counter's division value.

* The time actually set to the timer is adjusted by adding the time described above to the communication time for the serial data transfer clock used for the setting.

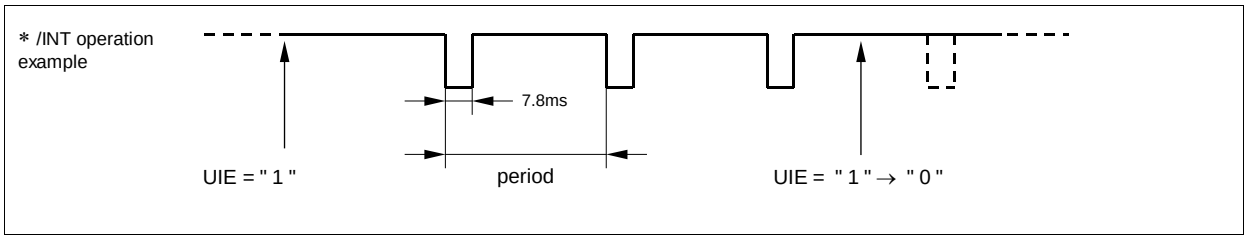
8.3.4. Fixed-cycle timer start timing

Counting down of the fixed-cycle timer value starts at the rising edge of the SCL signal that occurs when the TE value is changed from "0" to "1" (after bit 0 is transferred).

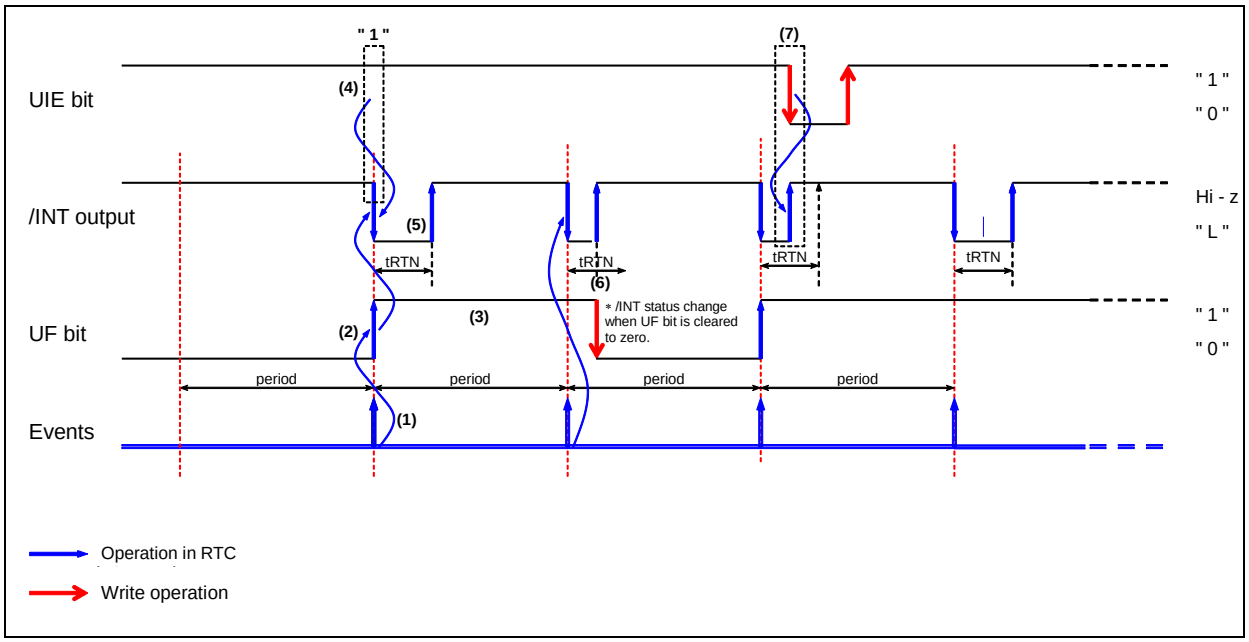


## 8.4. Time Update Interrupt Function

The time update interrupt function generates interrupt events at one-second or one-minute intervals, according to the timing of the internal clock.
When an interrupt event occurs, the UF bit value becomes "1" and the /INT pin goes to low level to indicate that an event has occurred. (However, when a fixed-cycle timer interrupt event has been generated, low-level output from the /INT pin occurs only when the value of the control register's UIE bit is "1". This /INT status is automatically cleared (/INT status changes from low level to Hi-Z) 7.8 ms (fixed value) after the interrupt occurs.




### 8.4.1. Time update interrupt function diagram




(1) A time update interrupt event occurs when the internal clock's value matches either the second update time or the minute update time. The USEL bit's specification determines whether it is the second update time or the minute update time that must be matched.

(2) When a time update interrupt event occurs, the UF bit value becomes "1".

(3) When the UF bit value is "1" its value is retained until it is cleared to zero.

(4) When a time update interrupt occurs, /INT pin output is low if UIE = "1".
∗ If UIE = "0" when a timer update interrupt occurs, the /INT pin status remains Hi-Z.

(5) Each time an event occurs, /INT pin output is low only up to the tRTN time (which is fixed as 7.1825 ms for time update interrupts) after which it is automatically cleared to Hi-Z.
∗ /INT pin output goes low again when the next interrupt event occurs.

(6) When /INT = low, the /INT pin status changes from low to Hi-Z as soon as the UF bit value changes from "1" to "0".

(7) When /INT = low, the /INT pin status changes from low to Hi-Z as soon as the UIE bit value changes from "1" to "0".

8.4.2. Related registers for time update interrupt functions.

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0D, 1D | Extension Register | TEST | WADA | **USEL** | TE | FSEL1 | FSEL0 | TSEL1 | TSEL0 |
| 0E, 1E | Flag Register | ○ | ○ | **UF** | TF | AF | EVF | VLF | VDET |
| 0F, 1F | Control Register | CSEL1 | CSEL0 | **UIE** | TIE | AIE | EIE | ○ | RESET |

*) "o" indicates write-protected bits. A zero is always read from these bits.

* Before entering settings for operations, we recommend writing a "0" to the UIE bit to prevent hardware interrupts from occurring inadvertently while entering settings.

* When the RESET bit value is "1" time update interrupt events do not occur.

* Although the time update interrupt function cannot be fully stopped, if "0" is written to the UIE bit, the time update interrupt function can be prevented from changing the /INT pin status to low.

1) USEL (Update Interrupt Select) bit
This bit is used to select "second" update or "minute" update as the timing for generation of time update interrupt events.

| **USEL** | Data | Description |
|---|---|---|
| Write/Read | 0 | Selects "second update" (once per second) as the timing for generation of interrupt events |
| | 1 | Selects "minute update" (once per minute) as the timing for generation of interrupt events |

2) UF (Update Flag) bit
Once it has been set to "0", this flag bit value changes from "0" to "1" when a time update interrupt event occurs. When this flag bit = "1" its value is retained until a "0" is written to it.

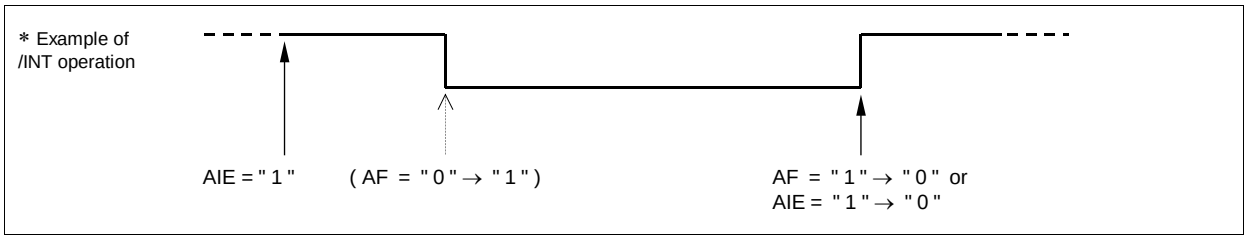
| **UF** | Data | Description |
|---|---|---|
| Write | 0 | The UF bit is cleared to zero to prepare for the next status detection<br>* Clearing this bit to zero does not enable the /INT low output status to be cleared (to Hi-Z). |
| | 1 | This bit is invalid after a "1" has been written to it. |
| Read | 0 | Time update interrupt events are not detected. |
| | 1 | Time update interrupt events are detected.<br>(The result is retained until this bit is cleared to zero.) |

3) UIE (Update Interrupt Enable) bit
When a time update interrupt event occurs (UF bit value changes from "0" to "1"), this bit selects whether to generate an interrupt signal (/INT status changes from Hi-Z to low) or to not generate it (/INT status remains Hi-Z).

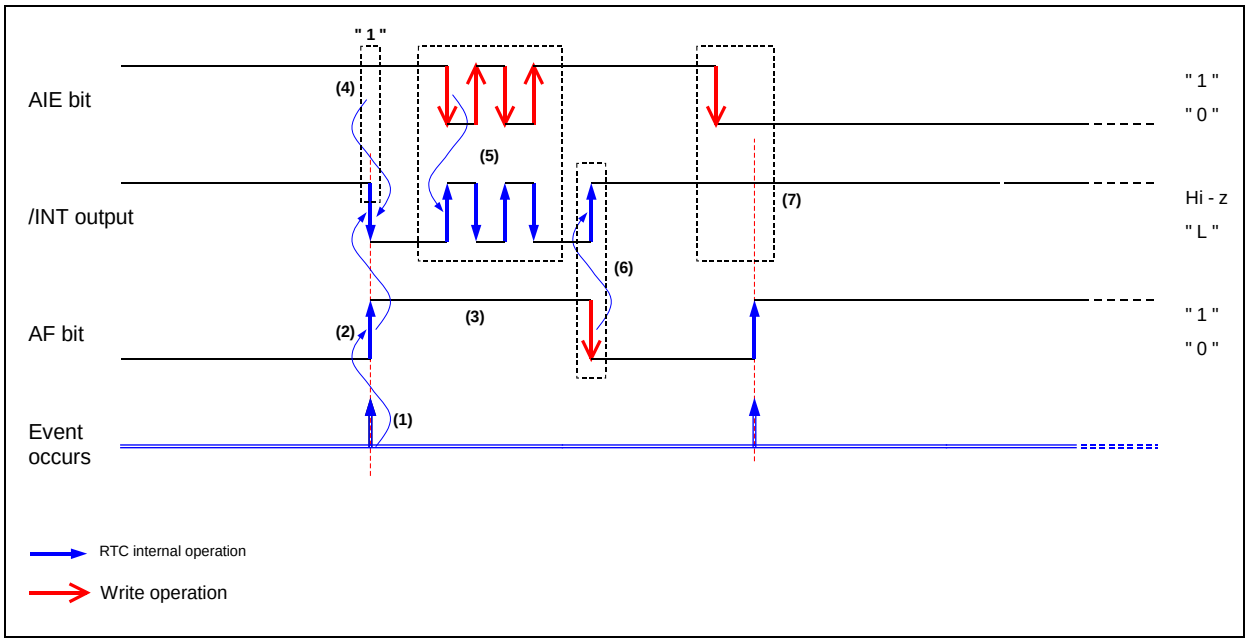
| **UIE** | Data | Description |
|---|---|---|
| Write/Read | 0 | 1) Does not generate an interrupt signal when a time update interrupt event occurs (/INT remains Hi-Z)<br>2) Cancels interrupt signal triggered by time update interrupt event (/INT changes from low to Hi-Z).<br>* Even when the UIE bit value is "0" another interrupt event may change the /INT status to low (or may hold /INT = "L"). |
| | 1 | When a time update interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low).<br>* When a time update interrupt event occurs, low-level output from the /INT pin occurs only when the UIE bit value is "1". Up to 7.8 ms after the interrupt occurs, the /INT status is automatically cleared (/INT status changes from low to Hi-Z). |

## 8.5. Alarm Interrupt Function

The alarm interrupt generation function generates interrupt events for alarm settings such as date, day, hour, and minute settings.
When an interrupt event occurs, the AF bit value is set to "1" and the /INT pin goes to low level to indicate that an event has occurred.




### 8.4.1. Diagram of alarm interrupt function




(1) The hour, minute, date or day when an alarm interrupt event is to occur is set in advance along with the WADA bit, and when the setting matches the current time an interrupt event occurs.
(Note) Even if the current date/time is used as the setting, the alarm will not occur until the counter counts up to the current date/time (i.e., an alarm will occur next time, not immediately).

(2) When a time update interrupt event occurs, the AF bit values becomes "1".

(3) When the AF bit = "1", its value is retained until it is cleared to zero.

(4) If AIE = "1" when an alarm interrupt occurs, the /INT pin output goes low.
* When an alarm interrupt event occurs, /INT pin output goes low, and this status is then held until it is cleared via the AF bit or AIE bit.

(5) If the AIE value is changed from "1" to "0" while /INT is low, the /INT status immediately changes from low to Hi-Z. After the alarm interrupt occurs and before the AF bit value is cleared to zero, the /INT status can be controlled via the AIE bit.

(6) If the AF bit value is changed from "1" to "0" while /INT is low, the /INT status immediately changes from low to Hi-Z.

(7) If the AIE bit value is "0" when an alarm interrupt occurs, the /INT pin status remains Hi-Z.

8.5.2. Related registers

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 01, 12 | MIN | ○ | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| 02, 13 | HOUR | ○ | ○ | 20 | 10 | 8 | 4 | 2 | 1 |
| 03, 14 | WEEK | ○ | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 04, 15 | DAY | ○ | ○ | 20 | 10 | 8 | 4 | 2 | 1 |
| 08, 18 | MIN Alarm | **AE** | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| 09, 19 | HOUR Alarm | **AE** | • | 20 | 10 | 8 | 4 | 2 | 1 |
| 0A, 1A | WEEK Alarm | **AE** | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | DAY Alarm | | • | 20 | 10 | 8 | 4 | 2 | 1 |
| 0D, 1D | Extension Register | TEST | WADA | USEL | TE | FSEL1 | FSEL0 | TSEL1 | TSEL0 |
| 0E, 1E | Flag Register | ○ | ○ | UF | TF | **AF** | EVF | VLF | VDET |
| 0F, 1F | Control Register | CSEL1 | CSEL0 | UIE | TIE | **AIE** | EIE | ○ | RESET |

∗1) "o" indicates write-protected bits. A zero is always read from these bits.

∗2) Bits marked with "•" are RAM bits that can contain any value and are read/write-accessible.

∗ Before entering settings for operations, we recommend writing a "0" to the AIE bit to prevent hardware interrupts from occurring inadvertently while entering settings.

∗ When the RESET bit value is "1" alarm interrupt events do not occur.

∗ When the alarm interrupt function is not being used, the Alarm registers (Reg - 8 to A) can be used as a RAM register. In such cases, be sure to write "0" to the AIE bit.

∗ When the AIE bit value is "1" and the Alarm registers (Reg - 8 to A) is being used as a RAM register, /INT may be changed to low level unintentionally.

1) WADA (Week Alarm /Day Alarm) bit

The alarm interrupt function uses either "Day" or "Week" as its target. The WADA bit is used to specify either WEEK or DAY as the target for alarm interrupt events.

| **WADA** | Data | Description |
|---|---|---|
| Write/Read | 0 | Sets WEEK as target of alarm function<br>(DAY setting is ignored) |
| | 1 | Sets DAY as target of alarm function<br>(WEEK setting is ignored) |

2) Alarm registers

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 08, 18 | MIN Alarm | AE | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| 09, 19 | HOUR Alarm | AE | • | 20 | 10 | 8 | 4 | 2 | 1 |
| 0A,1A | WEEK Alarm | AE | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | DAY Alarm | | • | 20 | 10 | 8 | 4 | 2 | 1 |

The hour, minute, date or day when an alarm interrupt event will occur is set using this register and the WADA bit.

In the WEEK alarm /Day alarm register (Reg - A), the setting selected via the WADA bit determines whether WEEK alarm data or DAY alarm data will be set. If WEEK has been selected via the WADA bit, multiple days can be set (such as Monday, Wednesday, Friday, Saturday).

When the settings made in the alarm registers and the WADA bit match the current time, the AF bit value is changed to "1". At that time, if the AIE bit value has already been set to "1", the /INT pin goes low.

∗1) The register that "1" was set to "AE" bit, doesn't compare alarm.
(Example) Write 80h (AE = "1") to the WEEK Alarm /DAY Alarm register (Reg - A):
Only the hour and minute settings are used as alarm comparison targets. The week and date settings are not used as alarm comparison targets.
As a result, alarm occurs if only an hour and minute accords with alarm data.

∗2) If all three AE bit values are "1" the week/date settings are ignored and an alarm interrupt event will occur once per minute.

3) AF (Alarm Flag) bit

When this flag bit value is already set to "0", occurrence of an alarm interrupt event changes it to "1". When this flag bit value is "1", its value is retained until a "0" is written to it.

| **AF** | Data | Description |
|---|---|---|
| Write | 0 | The AF bit is cleared to zero to prepare for the next status detection<br>* Clearing this bit to zero enables /INT low output to be canceled (/INT remains Hi-Z) when an alarm interrupt event has occurred. |
| | 1 | This bit is invalid after a "1" has been written to it. |
| Read | 0 | Alarm interrupt events are not detected. |
| | 1 | Alarm interrupt events are detected.<br>(Result is retained until this bit is cleared to zero.) |

4) AIE (Alarm Interrupt Enable) bit

When an alarm interrupt event occurs (when the AF bit value changes from "0" to "1"), this bit's value specifies whether an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status remains Hi-Z).

| **AIE** | Data | Description |
|---|---|---|
| Write/Read | 0 | 1) When an alarm interrupt event occurs, an interrupt signal is not generated or is canceled (/INT status remains Hi-Z).<br>2) When an alarm interrupt event occurs, the interrupt signal is canceled (/INT status changes from low to Hi-Z).<br>* Even when the AIE bit value is "0" another interrupt event may change the /INT status to low (or may hold /INT = "L"). |
| | 1 | When an alarm interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low).<br>* When an alarm interrupt event occurs, low-level output from the /INT pin occurs only when the AIE bit value is "1". This value is retained (not automatically cleared) until the AF bit is cleared to zero. |

8.5.2. Examples of alarm settings

1) Example of alarm settings when "Day" has been specified (and WADA bit = "0")

| Day is specified<br>WADA bit = "0" | Reg – A bit 7 AE | bit 6 S | bit 5 F | bit 4 T | bit 3 W | bit 2 T | bit 1 M | bit 0 S | Reg - 9 HOUR Alarm | Reg - 8 MIN Alarm |
|---|---|---|---|---|---|---|---|---|---|---|
| Monday through Friday, at 7:00 AM<br>* Minute value is ignored | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 07 h | 80 h ~ FF h |
| Every Saturday and Sunday, for 30 minutes each hour * Hour value is ignored | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 80 h ~ FF h | 30 h |
| Every day, at 6:59 AM | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 18 h | 59 h |
| | 1 | X | X | X | X | X | X | X | | |

X: Don't care

2) Example of alarm settings when "Day" has been specified (and WADA bit = "1")

| Day is specified<br>WADA bit = "1" | Reg - A bit 7 AE | bit 6 • | bit 5 20 | bit 4 10 | bit 3 08 | bit 2 04 | bit 1 02 | bit 0 01 | Reg - 9 HOUR Alarm | Reg - 8 MIN Alarm |
|---|---|---|---|---|---|---|---|---|---|---|
| First of each month, at 7:00 AM<br>* Minute value is ignored | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 07 h | 80 h ~ FF h |
| 15th of each month, for 30 minutes each hour * Hour value is ignored | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 80 h ~ FF h | 30 h |
| Every day, at 6:59 PM | 1 | X | X | X | X | X | X | X | 18 h | 59 h |

X: Don't care

## 8.6. Reading/Writing Data via the I2C Bus Interface

### 8.6.1. Overview of I2C-BUS

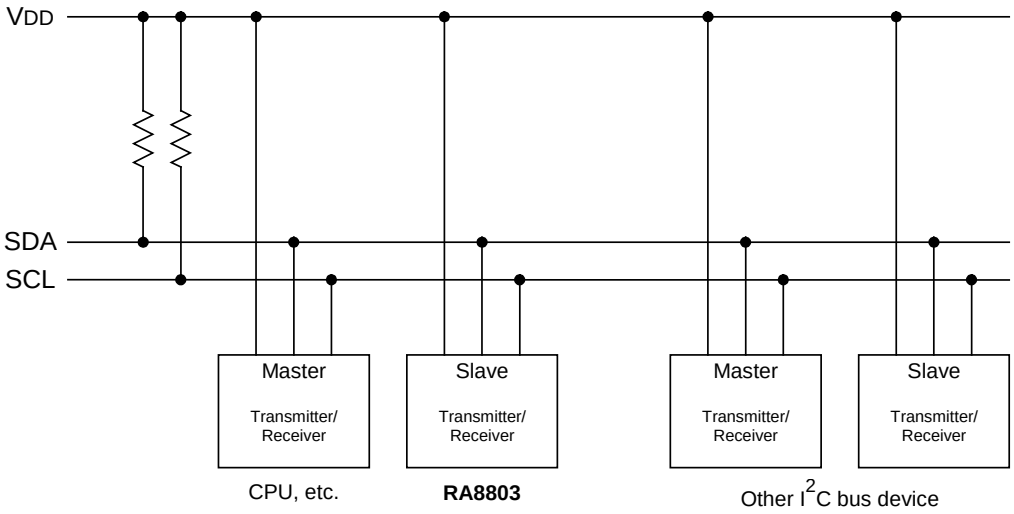
The I2C bus supports bi-directional communications via two signal lines: the SDA (data) line and SCL (clock) line. A combination of these two signals is used to transmit and receive communication start/stop signals, data transfer signals, acknowledge signals, and so on.

Both the SCL and SDA signals are held at high level whenever communications are not being performed.
The starting and stopping of communications is controlled at the rising edge or falling edge of SDA while SCL is at high level.

During data transfers, data changes that occur on the SDA line are performed while the SCL line is at low level, and on the receiving side the data is output while the SCL line is at high level.
The I2C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device and the receiving device responds to communications only when its slave address matches the slave address in the received data. In either case, the data is transferred via the SCL line at a rate of one bit per clock pulse.

### 8.6.2. System configuration

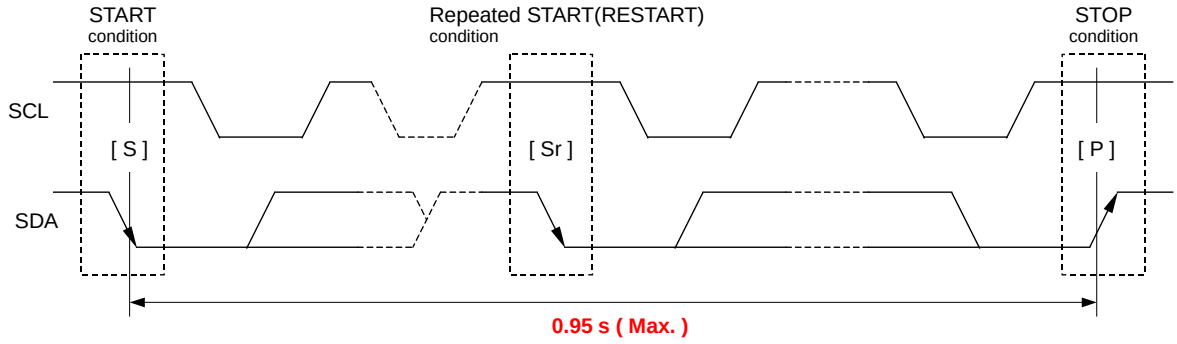
All ports connected to the I2C bus must be either open drain or open collector ports in order to enable AND connections to multiple devices.
SCL and SDA are both connected to the VDD line via a pull-up resistance. Consequently, SCL and SDA are both held at high level when the bus is released (when communication is not being performed).




Any device that controls the data transmission and data reception is defined as a "Master".
and any device that is controlled by a master device is defined as a “Slave”.
The device transmitting data is defined as a “Transmitter” and the device receiving data is defined as a receiver”

In the case of this RTC module, controllers such as a CPU are defined as master devices and the RTC module is defined as a slave device. When a device is used for both transmitting and receiving data, it is defined as either a transmitter or receiver depending on these conditions.

8.6.3. Starting and stopping $I^2C$ bus communications




1) START condition, repeated START condition, and STOP condition

(1) START condition

- The SDA level changes from high to low while SCL is at high level.

(2) STOP condition

- This condition regulates how communications on the $I^2C$-BUS are terminated. The SDA level changes from low to high while SCL is at high level.

(3) Repeated START condition (RESTART condition)

- In some cases, the START condition occurs between a previous START condition and the next STOP condition, in which case the second START condition is distinguished as a RESTART condition. Since the required status is the same as for the START condition, the SDA level changes from high to low while SCL is at high level.

2) Caution points

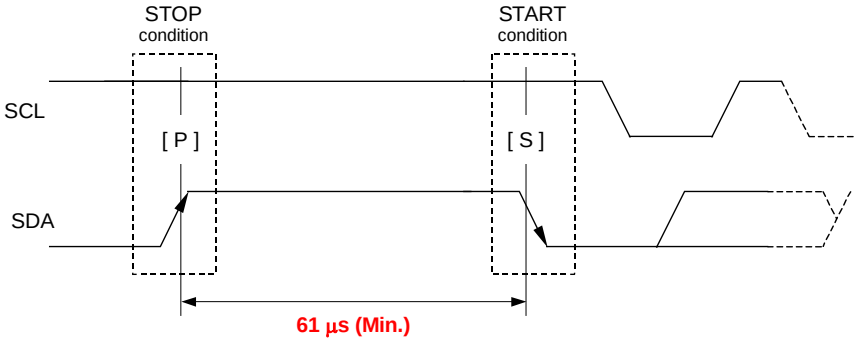
∗1) The master device always controls the START, RESTART, and STOP conditions for communications.

∗2) The master device does not impose any restrictions on the timing by which STOP conditions affect transmissions, so communications can be forcibly stopped at any time while in progress. (However, this is only when this RTC module is in receiver mode (data reception mode = SDA released).

∗3) When communicating with this RTC module, the series of operations from transmitting the START condition to transmitting the STOP condition should occur **within 0.95 seconds**. (A RESTART condition may be sent between a START condition and STOP condition, but even in such cases the series of operations from transmitting the START condition to transmitting the STOP condition should still occur **within 0.95 seconds**.)

If this series of operations requires **0.95 seconds or longer,** the $I^2C$ bus interface will be automatically cleared and set to standby mode by this RTC module's bus timeout function. Note with caution that both write and read operations are invalid for communications that occur during or after this auto clearing operation. (When the read operation is invalid, all data that is read has a value of "1").
Restarting of communications begins with transfer of the START condition again

∗4) When communicating with this RTC module, wait **at least 1.3 µs (see the tBUF rule)** between transferring a STOP condition (to stop communications) and transferring the next START condition (to start the next round of communications).



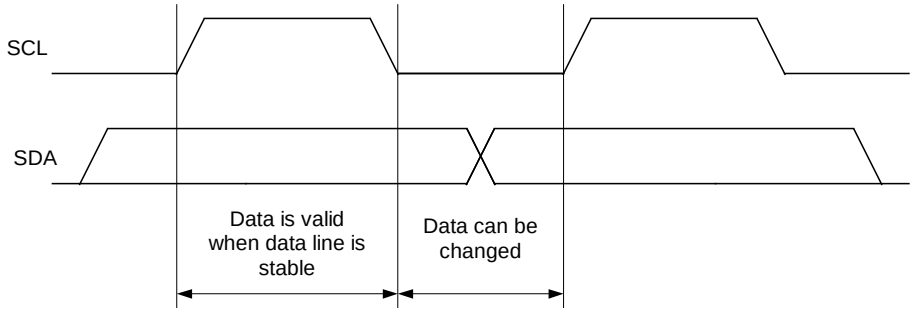
8.6.4. Data transfers and acknowledge responses during I²C-BUS communications

1) Data transfers

Data transfers are performed in 8-bit (1 byte) units once the START condition has occurred. There is no limit on the amount (bytes) of data that are transferred between the START condition and STOP condition. (**However, the transfer time must be no longer than 0.95 seconds**.)

The address auto increment function operates during both write and read operations.
**After address Fh, incrementation goes to address 0h**.

Updating of data on the transmitter (transmitting side)'s SDA line is performed while the SCL line is at low level. The receiver (receiving side) receives data while the SCL line is at high level.

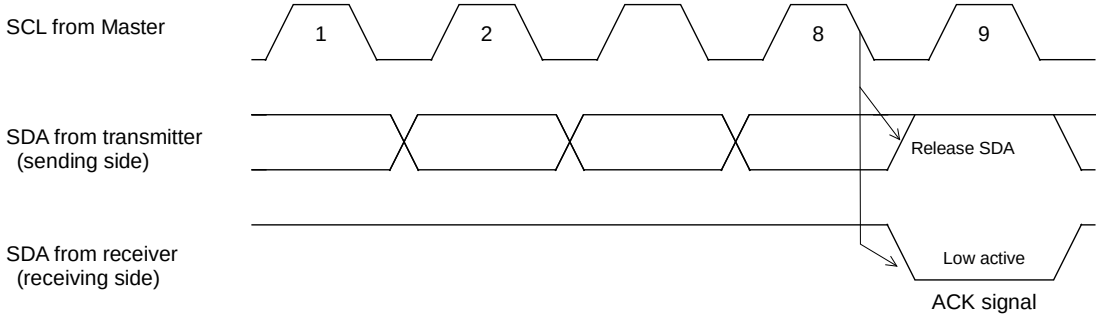



∗ Note with caution that if the SDA data is changed while the SCL line is at high level, it will be treated as a START, RESTART, or STOP condition.

2) Data acknowledge response (ACK signal)

When transferring data, the receiver generates a confirmation response (ACK signal, low active) each time an 8-bit data segment is received. If there is no ACK signal from the receiver, it indicates that normal communication has not been established. (This does not include instances where the master device intentionally does not generate an ACK signal.)

Immediately after the falling edge of the clock pulse corresponding to the 8th bit of data on the SCL line, the transmitter releases the SDA line and the receiver sets the SDA line to low (= acknowledge) level.




After transmitting the ACK signal, if the Master remains the receiver for transfer of the next byte, the SDA is released at the falling edge of the clock corresponding to the 9th bit of data on the SCL line. Data transfer resumes when the Master becomes the transmitter.
When the Master is the receiver, if the Master does not send an ACK signal in response to the last byte sent from the slave, that indicates to the transmitter that data transfer has ended. At that point, the transmitter continues to release the SDA and awaits a STOP condition from the Master.

8.6.5. Slave address

The I²C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device.
All communications begin with transmitting the [START condition] + [slave address (+ R/W specification)]. The receiving device responds to this communication only when the specified slave address it has received matches its own slave address.

Slave addresses have a fixed length of 7 bits. This RTC's slave address is **[0110 010∗]**.
An R/W bit ("*" above) is added to each 7-bit slave address during 8-bit transfers.

| | Transfer data | Slave address | | | | | | | R/W bit |
|---|---|---|---|---|---|---|---|---|---|
| | | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| Read | **65 h** | **0** | **1** | **1** | **0** | **0** | **1** | **0** | 1 (= Read) |
| Write | **64 h** | | | | | | | | 0 (= Write) |

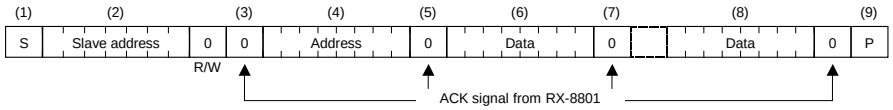
8.6.6. I²C bus protocol

In the following sequence descriptions, it is assumed that the CPU is the master and the RA8803 is the slave.

a. Address specification write sequence

Since the RA8803 includes an address auto increment function, once the initial address has been specified, the RA8803 increments (by one byte) the receive address each time data is transferred.

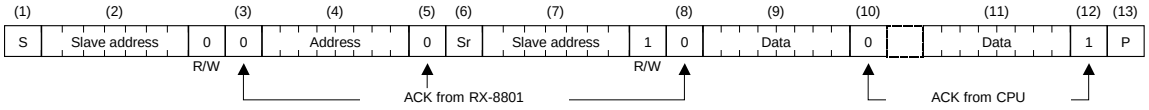
(1) CPU transfers start condition [S].
(2) CPU transmits the RA8803's slave address with the R/W bit set to write mode.
(3) Check for ACK signal from RA8803.
(4) CPU transmits write address to RA8803.
(5) Check for ACK signal from RA8803.
(6) CPU transfers write data to the address specified at (4) above.
(7) Check for ACK signal from RA8803.
(8) Repeat (6) and (7) if necessary. Addresses are automatically incremented.
(9) CPU transfers stop condition [P].




b. Address specification read sequence

After using write mode to write the address to be read, set read mode to read the actual data.

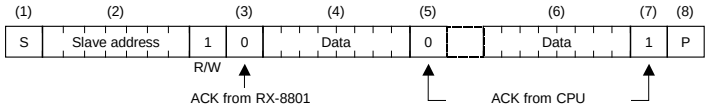
(1) CPU transfers start condition [S].
(2) CPU transmits the RA8803's slave address with the R/W bit set to write mode.
(3) Check for ACK signal from RA8803.
(4) CPU transfers address for reading from 8803.
(5) Check for ACK signal from RA8803.
(6) CPU transfers RESTART condition [Sr] (in which case, CPU does not transfer a STOP condition [P]).
(7) CPU transfers RA8803's slave address with the R/W bit set to read mode.
(8) Check for ACK signal from RA8803 (from this point on, the CPU is the receiver and the RA8803 is the transmitter).
(9) Data from address specified at (4) above is output by the RA8803.
(10) CPU transfers ACK signal to RA8803.
(11) Repeat (9) and (10) if necessary. Read addresses are automatically incremented.
(12) CPU transfers ACK signal for "1".
(13) CPU transfers stop condition [P].



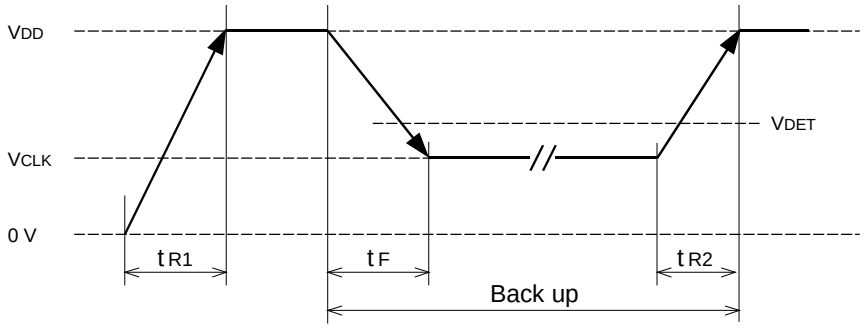

c. Read sequence when address is not specified

Once read mode has been initially set, data can be read immediately. In such cases, the address for each read operation is the previously accessed address + 1.

(1) CPU transfers start condition [S].
(2) CPU transmits the RA8803's slave address with the R/W bit set to read mode.
(3) Check for ACK signal from RA8803 (from this point on, the CPU is the receiver and the RA8803 is the transmitter).
(4) Data is output from the RA8803 to the address following the end of the previously accessed address.
(5) CPU transfers ACK signal to RA8803.
(6) Repeat (4) and (5) if necessary. Read addresses are automatically incremented in the RA8803.
(7) CPU transfers ACK signal for "1".
(8) CPU transfers stop condition [P].



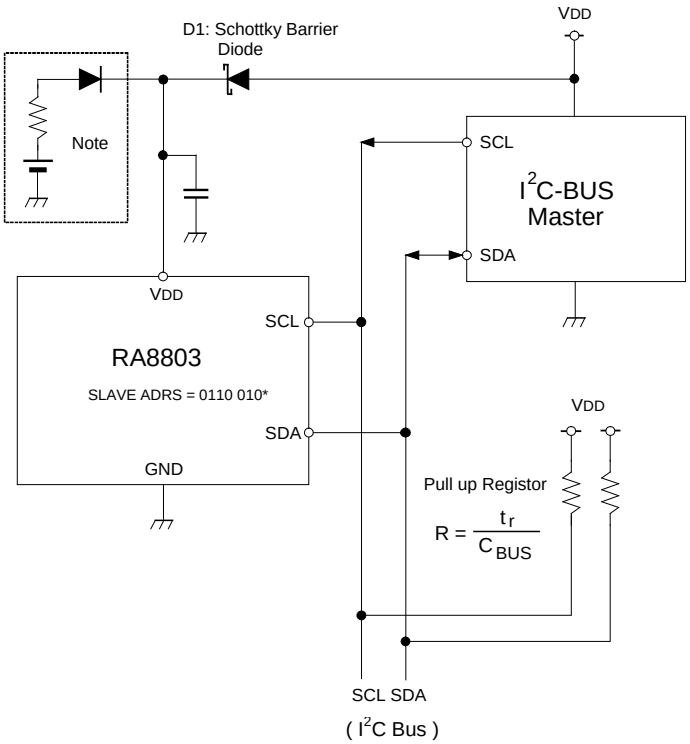
## 8.7. Backup and Recovery




| Item | Symbol | Condition | Min. | Typ. | Max. | Unit. |
|---|---|---|---|---|---|---|
| Power supply detection voltage ( 1 ) | $V_{DET}$ | – | | | 2.2 | V |
| Power supply detection voltage ( 2 ) | $V_{LOW}$ | – | | | 1.6 | V |
| Power supply drop time | $t_F$ | – | 2 | | | µs /V |
| Initial power-up time | $t_{R1}$ | – | | | 10 | ms /V |
| Clock maintenance power-up time | $t_{R2}$ | $1.6V \rightarrow V_{DD} \leq 3.6V$ | 5 | | | µs /V |
| | | $1.6V \rightarrow V_{DD} > 3.6V$ | 15 | | | µs /V |

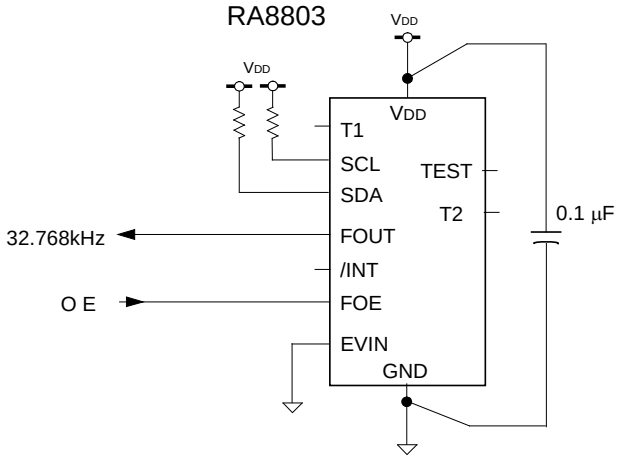
Please control a power supply in the above agreement so that normalcy operates a detect circuit of power supply injection.
Please start a power supply at 0V by all means.
Before power supply change operation and a shift to backup state , please set STOP condition.

## 8.8. Connection with Typical Microcontroller




Note : When using the seconding battery, the diode is not required.
When using the primary battery, the diode is required.
For detailed value on the resistance, please consult a battery maker.

## 8.9. When used as a clock source (32 kHz-TCXO)



## 8.10. Note about read-out method of a 1/100s register

RA-8803 is equipped with a 1/100s register.
As for 1/100 counters, it is worked in very fast clock than second.
Therefore, as for the count operation of each, behavior in a chip access hold facility (P.8 reference) operation is different.
When using a 1/100s register, be careful as follows.
Behavior, when access hold function worked.
When communication to a clock counter of an RTC started, by access hold facility, update in the time can stop hold automatically.
However, as for 1/100 second counters, data cannot stop hold, and count is continued.
As for 1/100 value, it is examined data by IC circuit, and it is captured to 1/100s register.

Therefore, there is case lost continuity of data in 1/100 second data and time data when 1/100 second digits are captured just after a second updates.

This phenomenon occurs in restrictive timing, but internal Time and date are correct and internal updates are correct.
A lag of a readout result is +1 second at the maximum.

Read-out method of 1/100 second digits to prevent mismatching of the time

Method 1

Method to read two times of 1/100 second digits

Step1: Please read 1/100 second digits and time data, and stored those.

Step2: Please read only 1/100 second digits again. Please complete Step2 within 10ms from Step1.

Step3: If two 1/100 second digits are same values, please goto next step.
If two values are different, please return to Step1.
Note
Between Step2 and Step1, please send STOP condition by all means. It is separate access.

Method 2

Method to use an interruption flag of the fixed period interrupt function.

Step1 Please clear USEL bit of address 0Dh or 1Dh in a zero. It is update interruption of sec.

Step2 Please clear UF bit of address Eh in a zero.

Step3 Please read time data and 1/100 data.

Step4 Please read UF bit.

Step5 Please adopt the data that reads in case of UF=0.
Please cancel the data that read in case of UF=1.

Step6 When it is executed again, return to Step2.

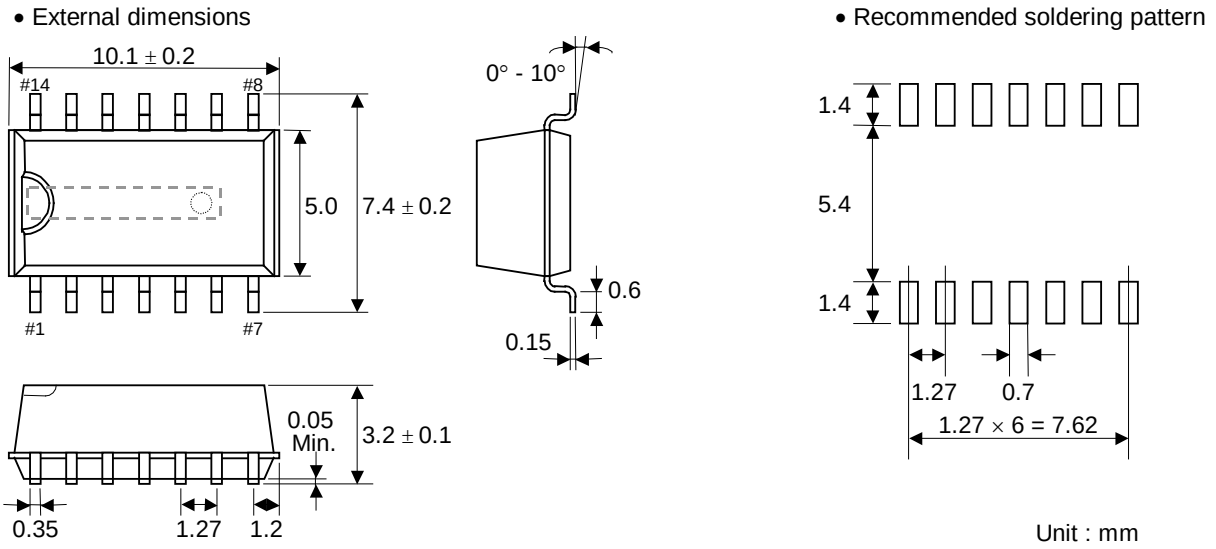
When second is updated, a UF bit is set to 1.
Therefore it must be executed Step2 and 4 within one second.
Please complete Step4 within 1sec from Step2.
(recommendation : lower than 10ms)
Please divide Step3 and Step4 by STOP condition. It is separate access.

# 9. External Dimensions / Marking Layout

## 9.1. RA8803 SA

### 9.1.1. External dimensions

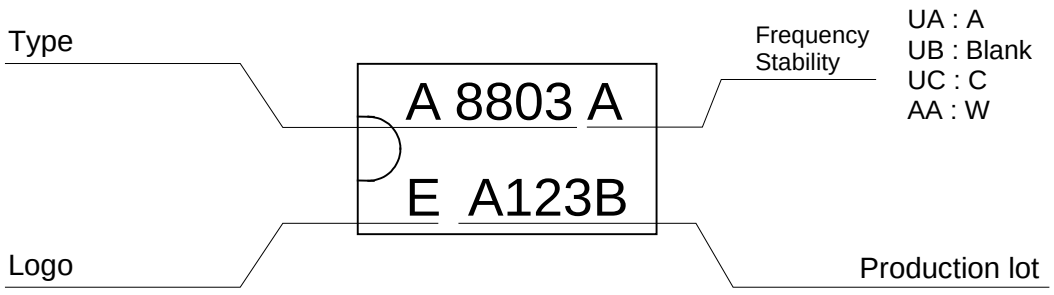
RA8803SA ( SOP – 14pin )




∗ The cylinder of the crystal oscillator can be seen in this area ( front ), but it has no affect on the performance of the device.

### 9.1.2. Marking layout

RA8803 SA ( SOP – 14pin )




∗ Contents displayed indicate the general markings and display, but are not the standards for the fonts, sizes and positioning.

# 10. Application notes

## 1) Notes on handling

This module uses a C-MOS IC to realize low power consumption. Carefully note the following cautions when handling.

(1) Static electricity

While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other such devices which do not leak high voltage should be used with this module, which should also be grounded when such devices are being used.

(2) Noise

If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up." In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of greater that 0.1 μF as close as possible to the power supply pins (between VDD and GNDs). Also, avoid placing any device that generates high level of electronic noise near this module.

* Do not connect signal lines to the shaded area in the figure shown in Fig. 1 and, if possible, embed this area in a GND land.

(3) Voltage levels of input pins

When the input pins are at the mid-level, this will cause increased current consumption and a reduced noise margin, and can impair the functioning of the device. Therefore, try as much as possible to apply the voltage level close to VDD or GND.

(4) Handling of unused pins

Since the input impedance of the input pins is extremely high, operating the device with these pins in the open circuit state can lead to unstable voltage level and malfunctions due to noise. Therefore, pull-up or pull-down resistors should be provided for all unused input pins.

## 2) Notes on packaging

(1) Soldering heat resistance.

If the temperature within the package exceeds +260 °C, the characteristics of the crystal oscillator will be degraded and it may be damaged. The reflow conditions within our reflow profile is recommended. Therefore, always check the mounting temperature and time before mounting this device. Also, check again if the mounting conditions are later changed.

* See Fig. 2 profile for our evaluation of Soldering heat resistance for reference.

(2) Mounting equipment

While this module can be used with general-purpose mounting equipment, the internal crystal oscillator may be damaged in some circumstances, depending on the equipment and conditions. Therefore, be sure to check this. In addition, if the mounting conditions are later changed, the same check should be performed again.

(3) Ultrasonic cleaning

Depending on the usage conditions, there is a possibility that the crystal oscillator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

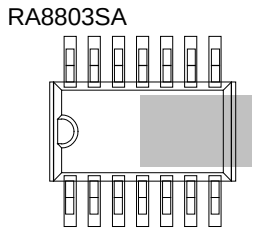
(4) Mounting orientation

This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

(5) Leakage between pins

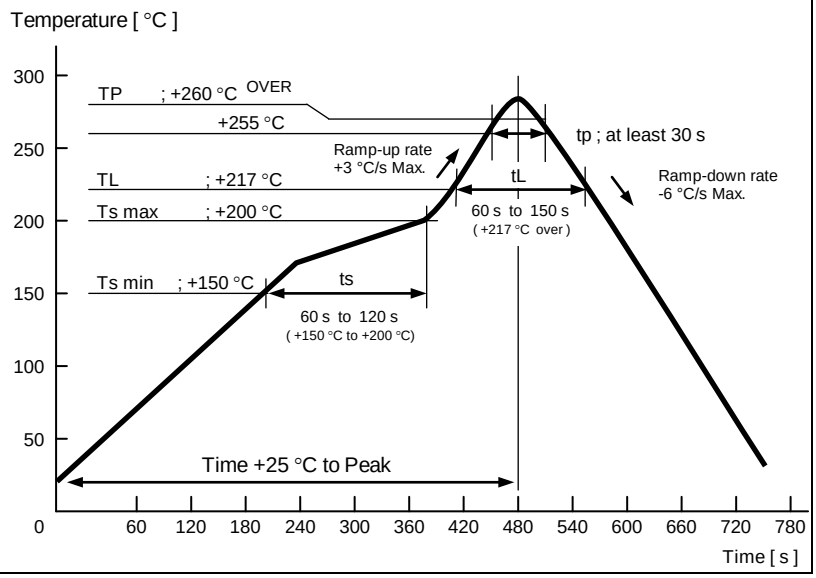
Leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.

Fig. 1 : Example GND Pattern




* The shaded part ( ) indicates where a GND pattern should be set without getting too close to a signal line

Fig. 2 : Reference profile for our evaluation of Soldering heat resistance.



# Application Manual

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